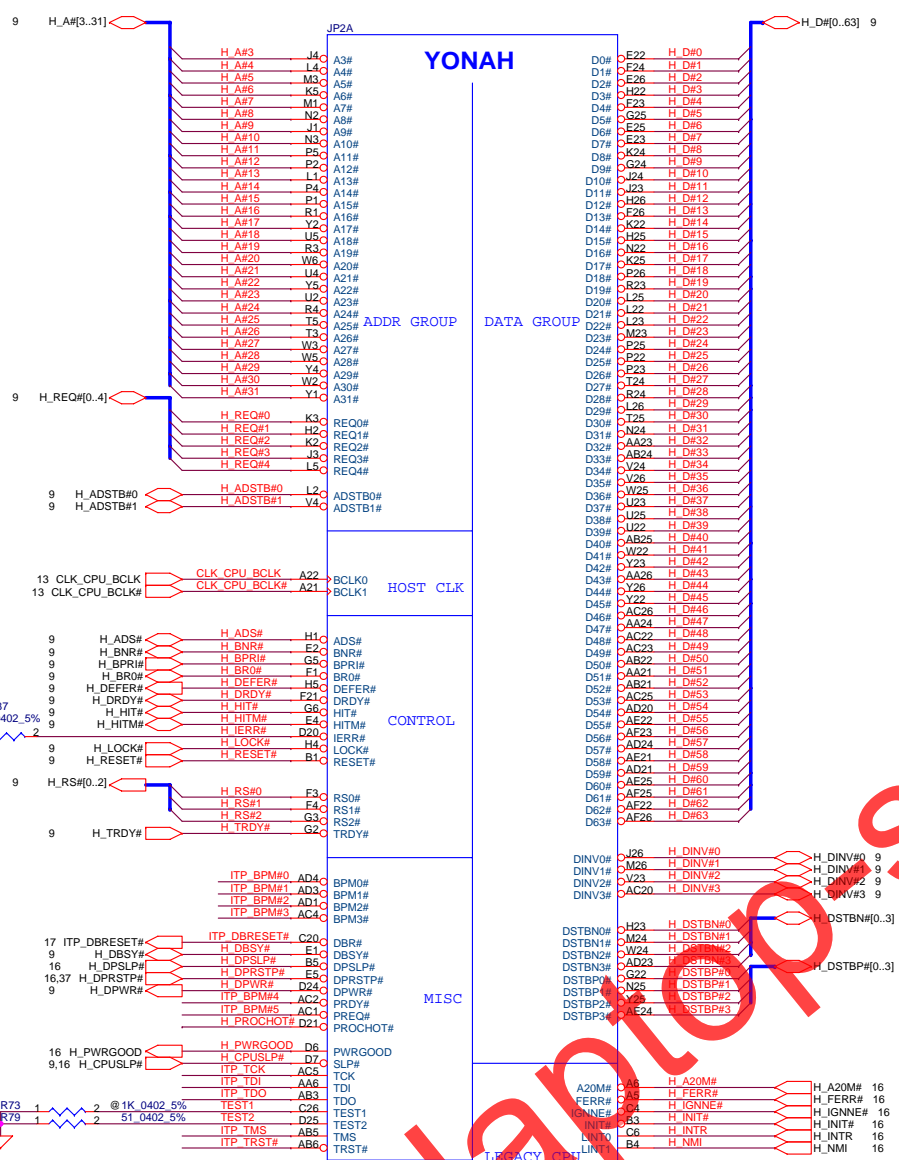
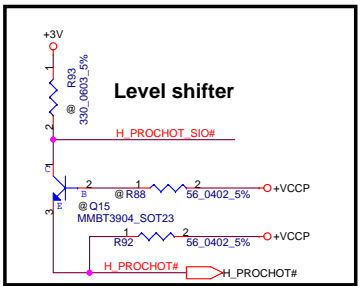
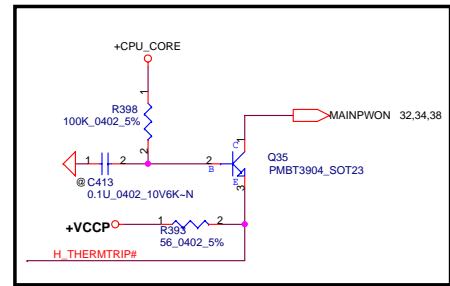
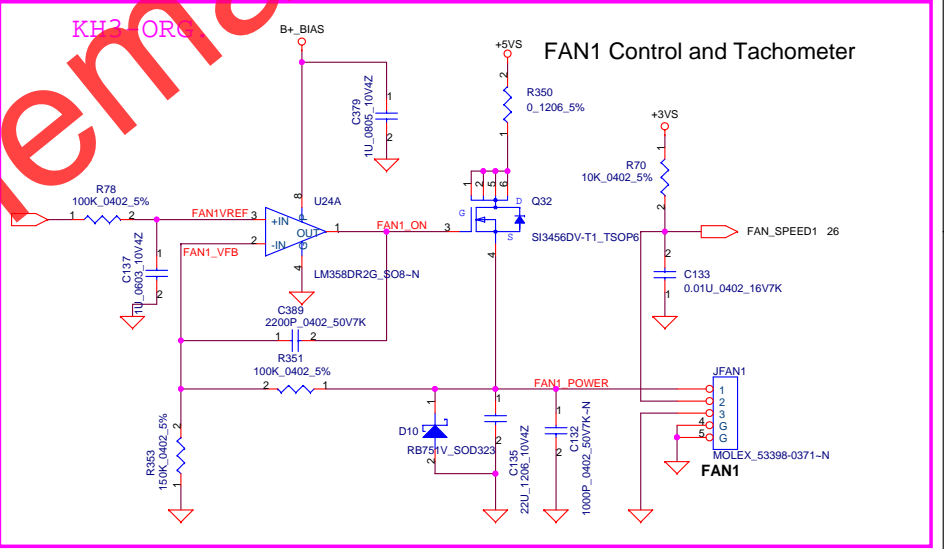
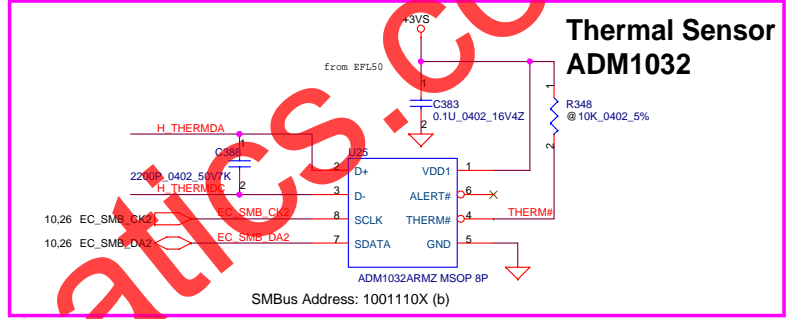
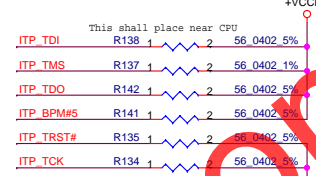
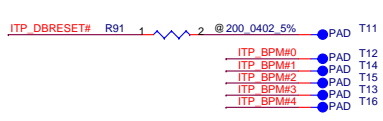
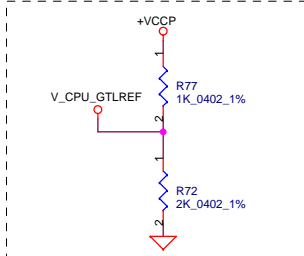


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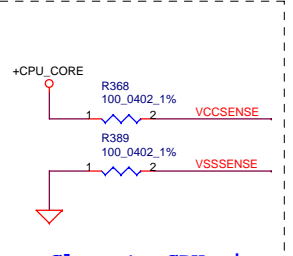


H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil





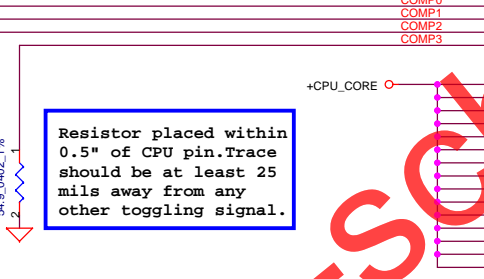
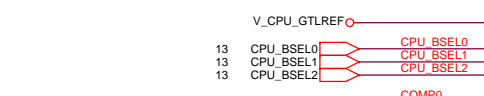
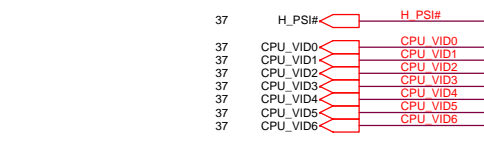
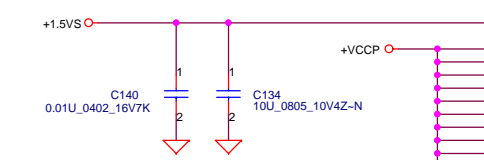
Close to CPU pin AD26 within 0.5 inch



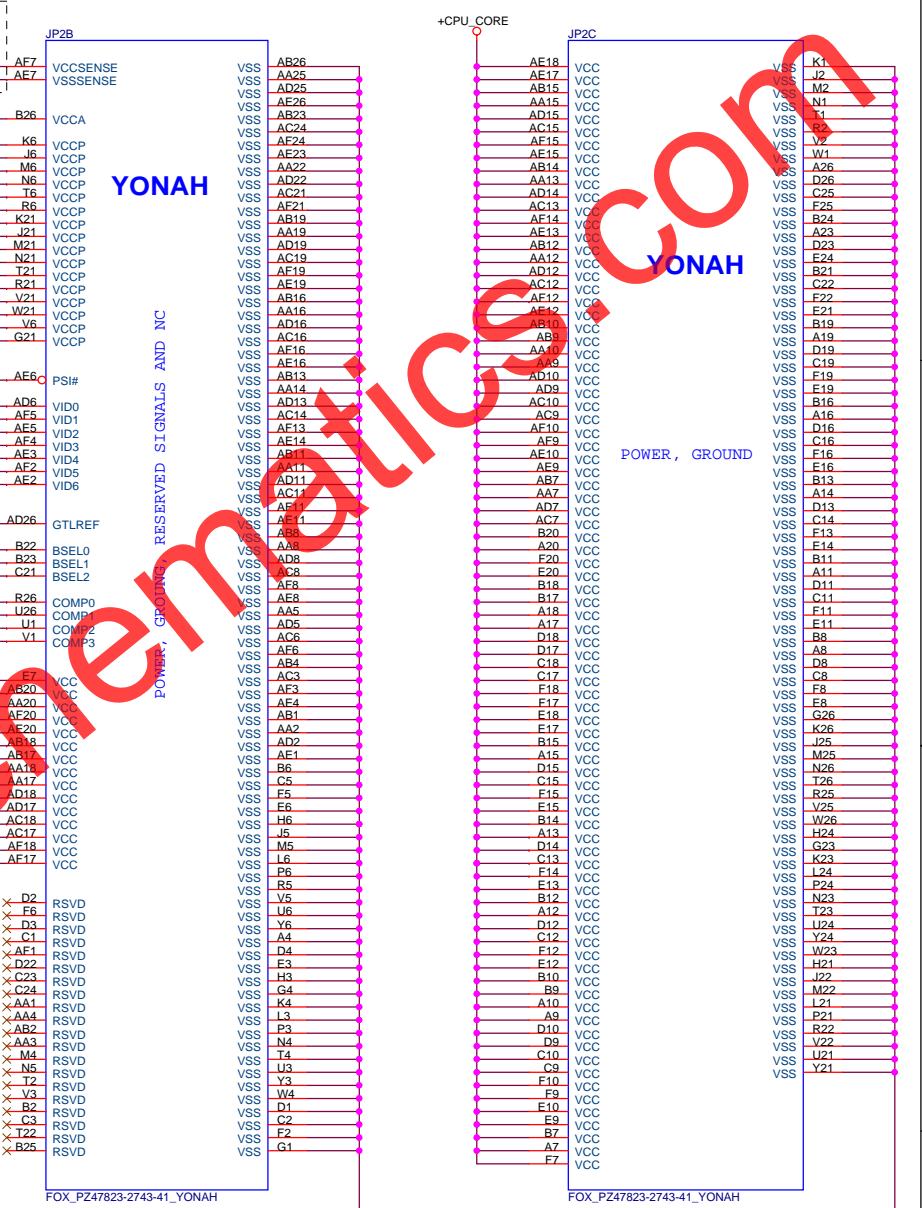
Close to CPU pin within 500mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Length match within 25 mils
The trace width 18 mils space
7 mils



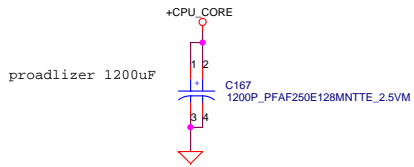
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



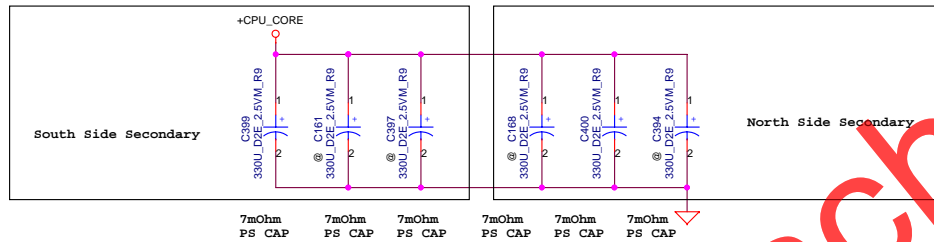
FOX_PZ47823-2743-41_YONAH

FOX_PZ47823-2743-41_YONAH

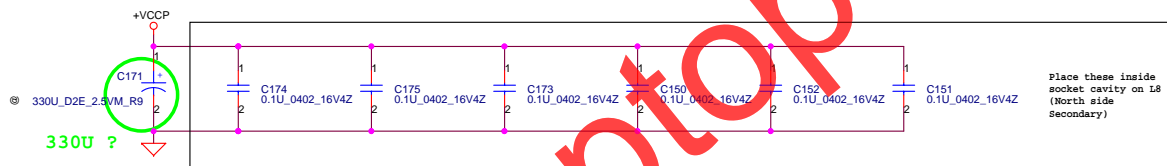
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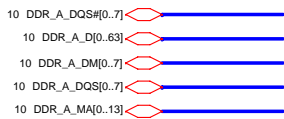
Mid Frequency Decoupling



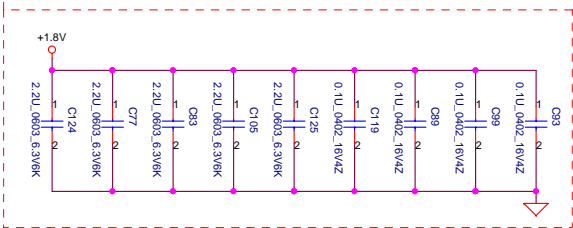
ESR <= 1.5m ohm
Capacitor > 1980uF



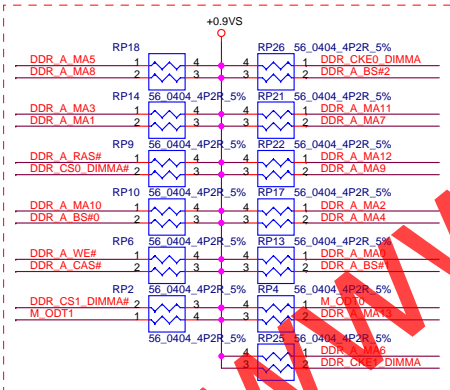
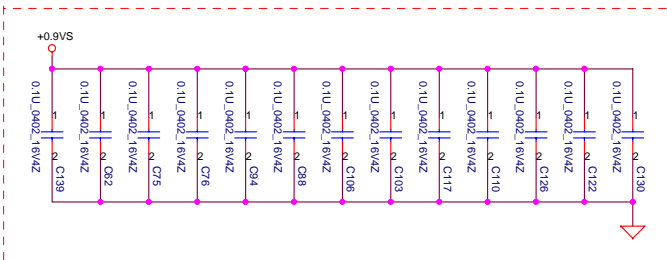
www.laptop-schematics.com



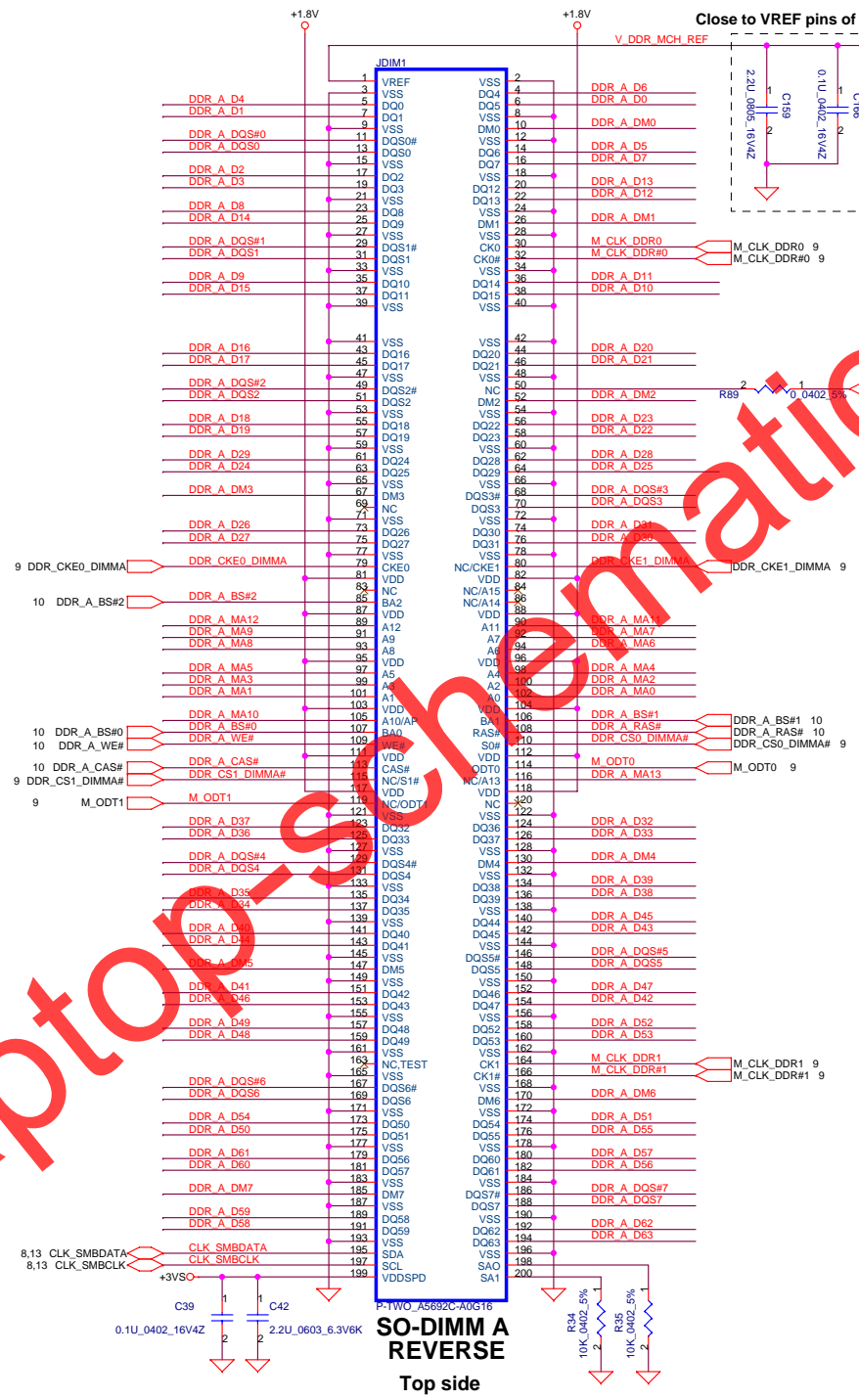
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

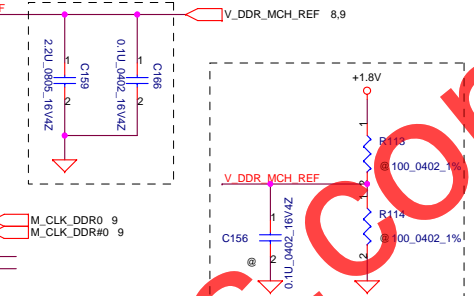


Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

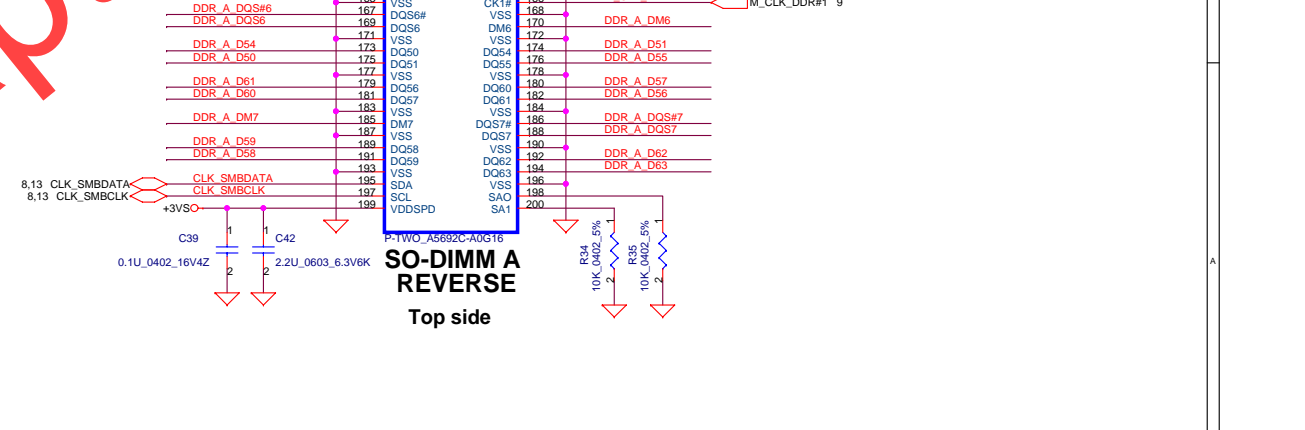


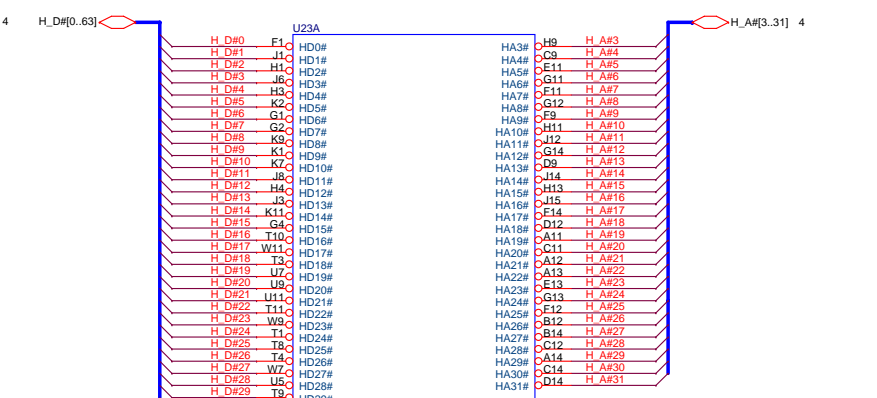
SO-DIMM A REVERSE
Top side

Close to VREF pins of SO-DIMM

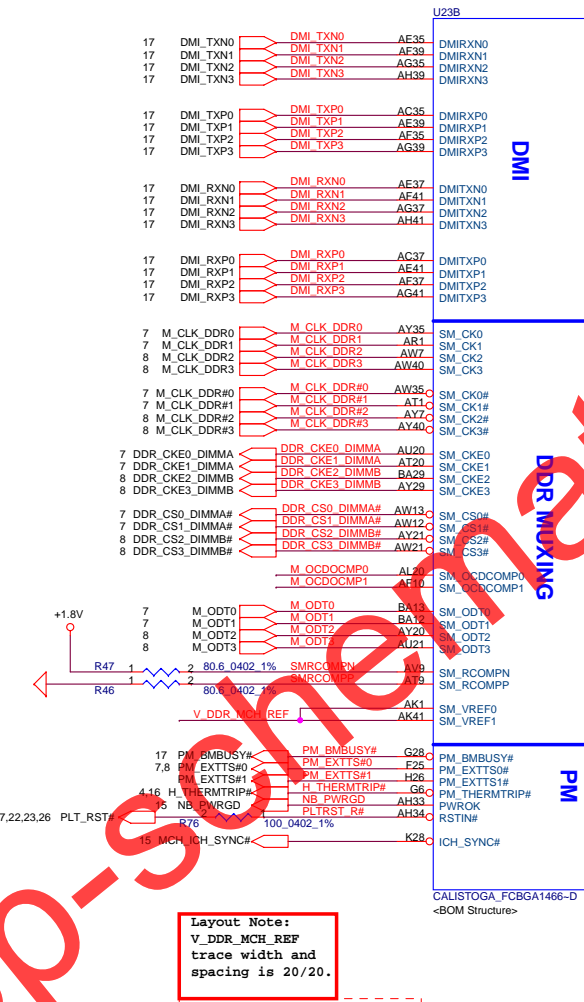
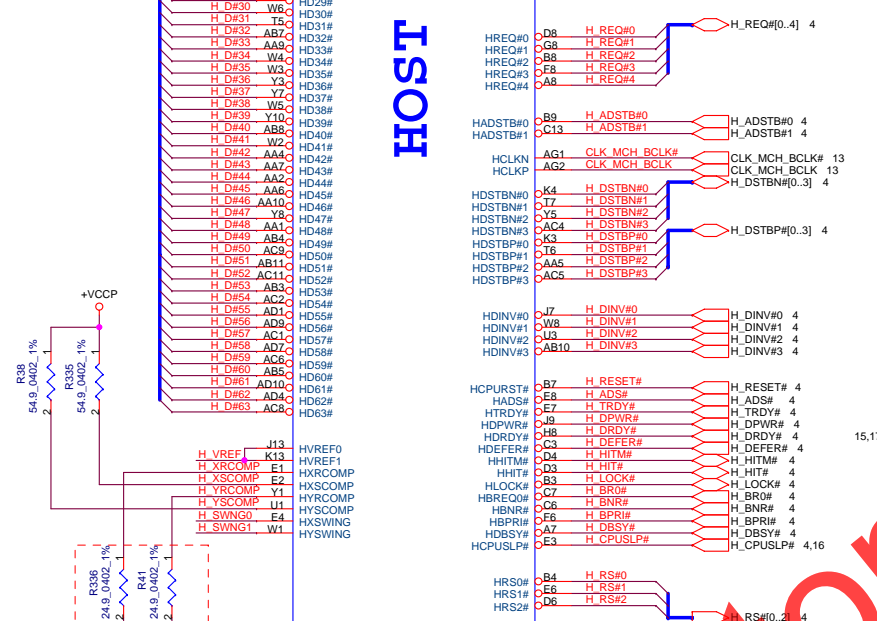


Close to connect

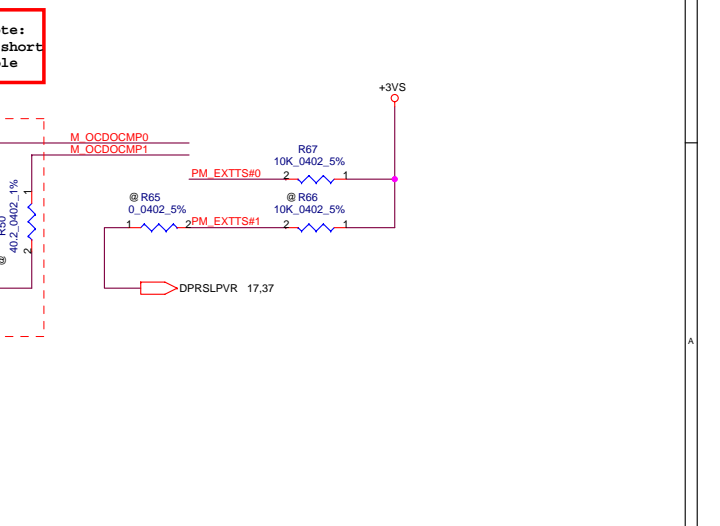
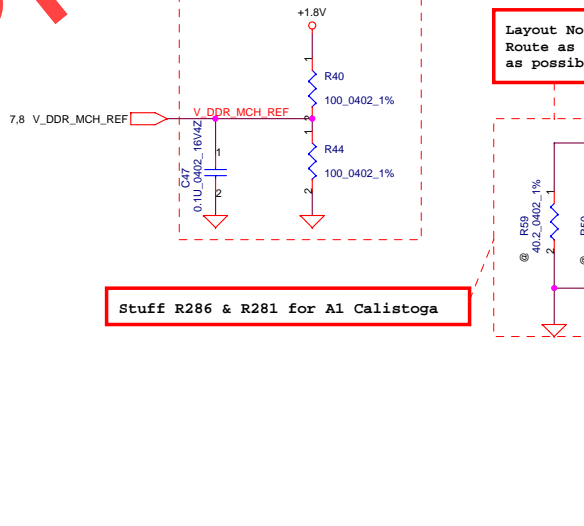
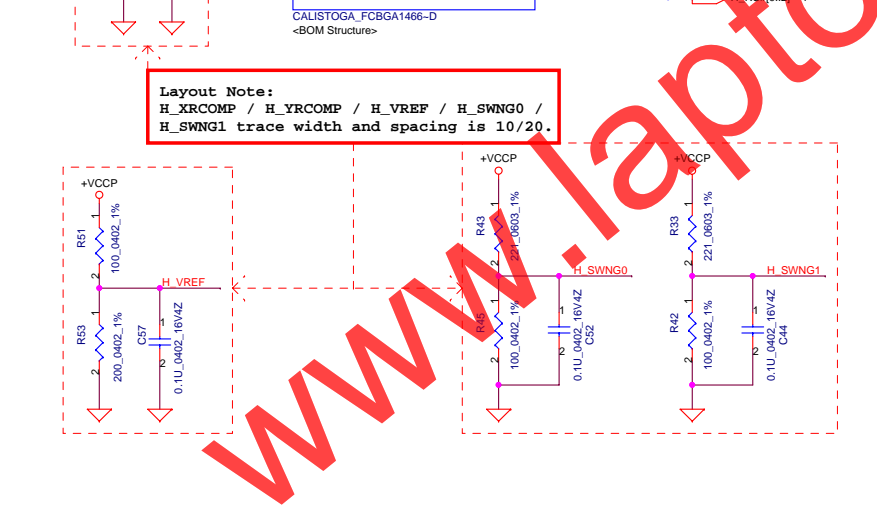




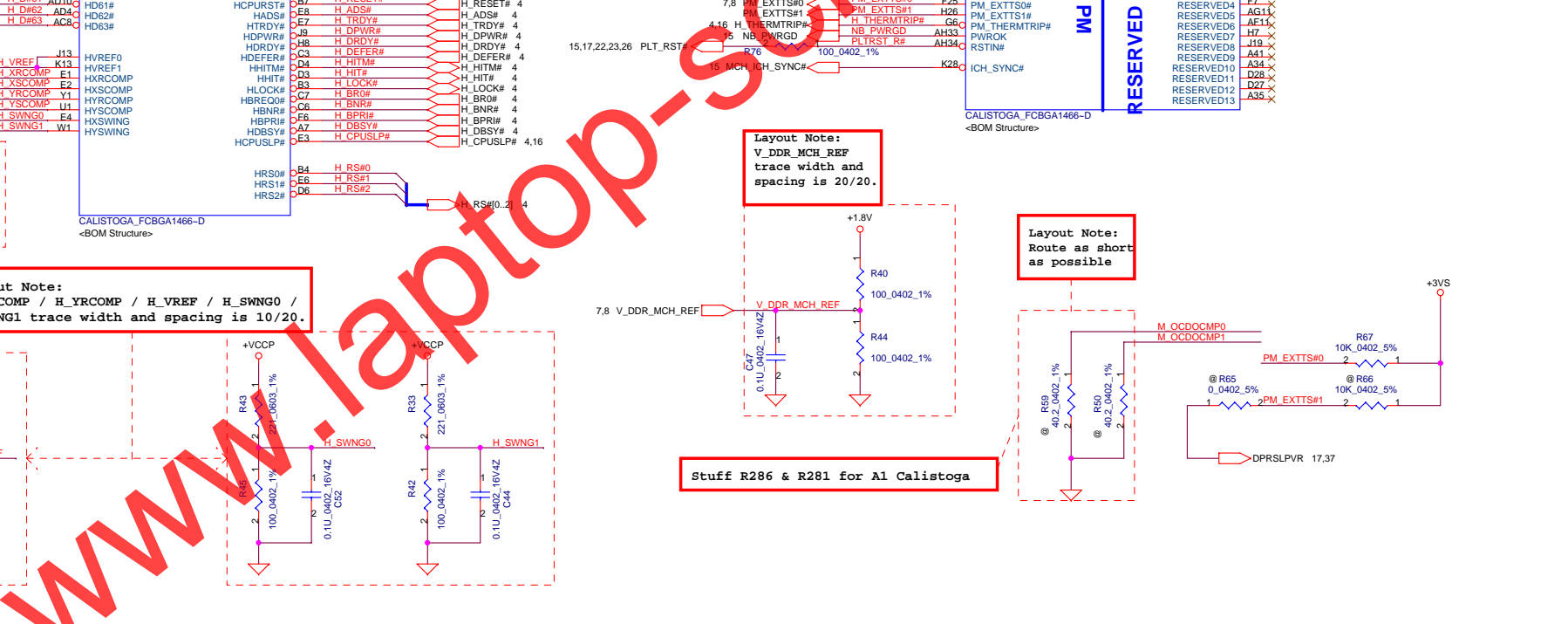
HOST

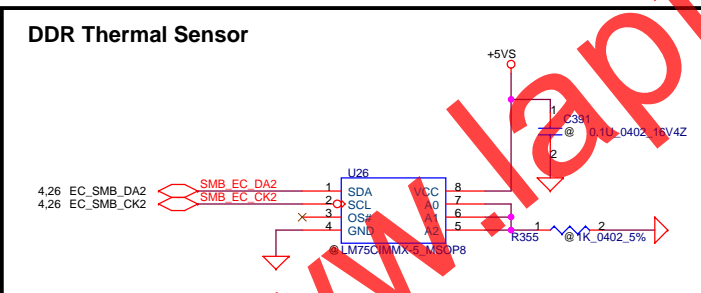
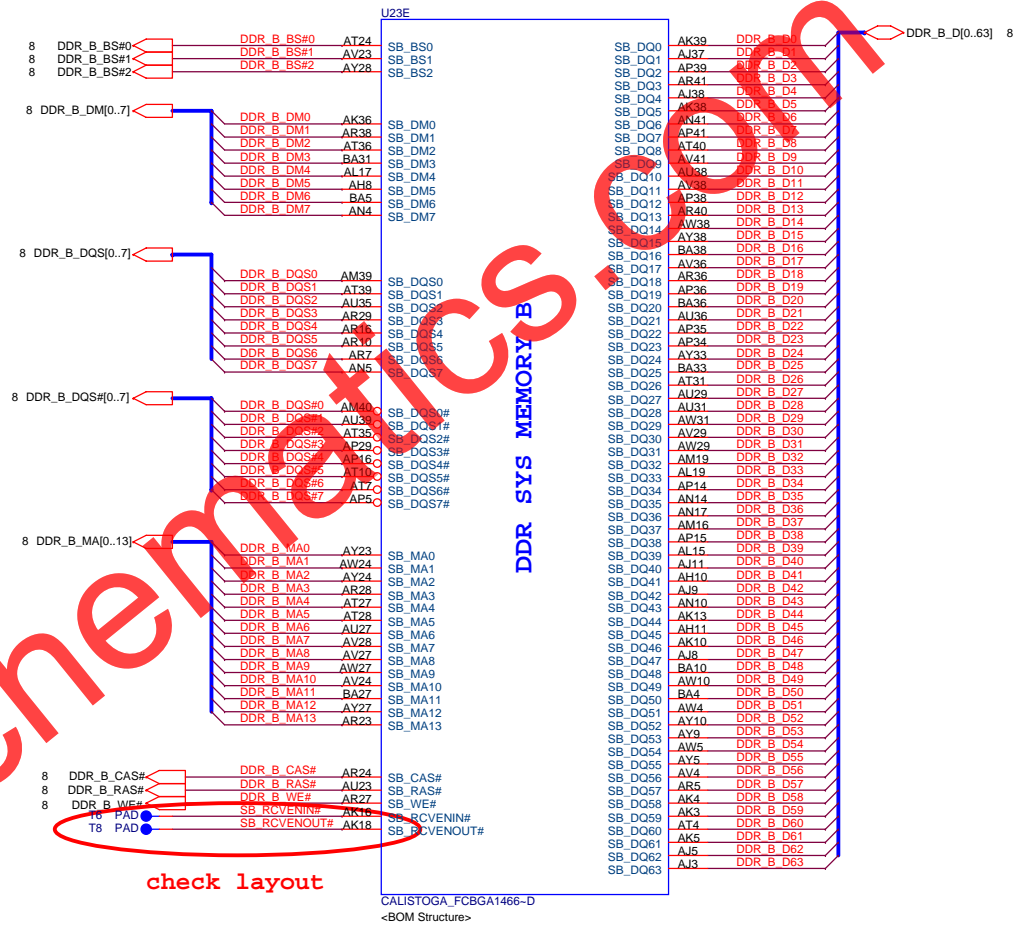


Description at pagel3.

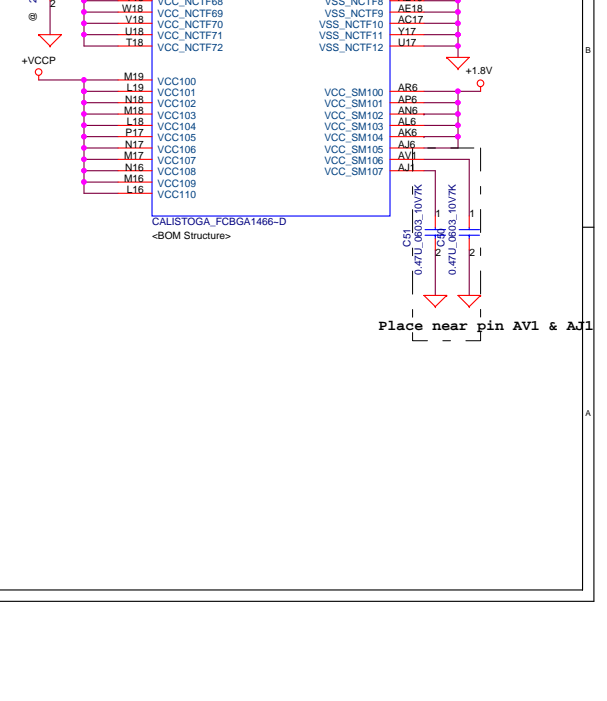
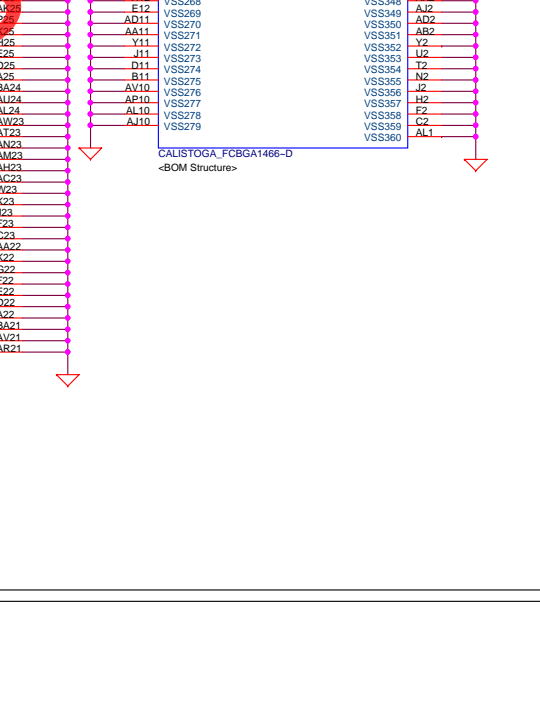
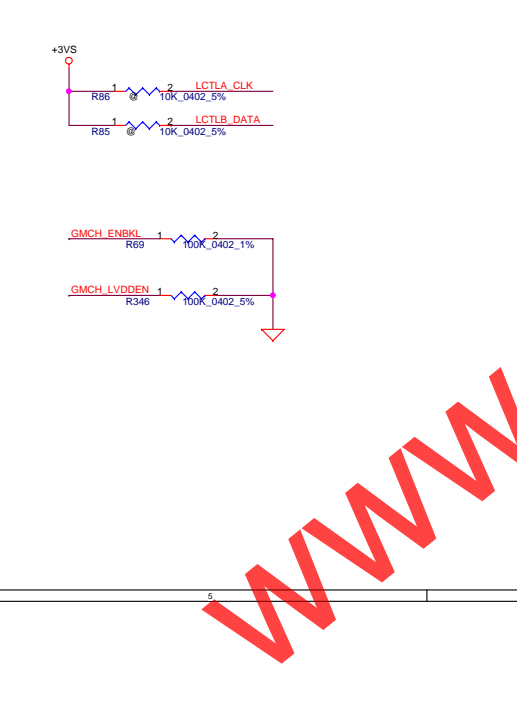
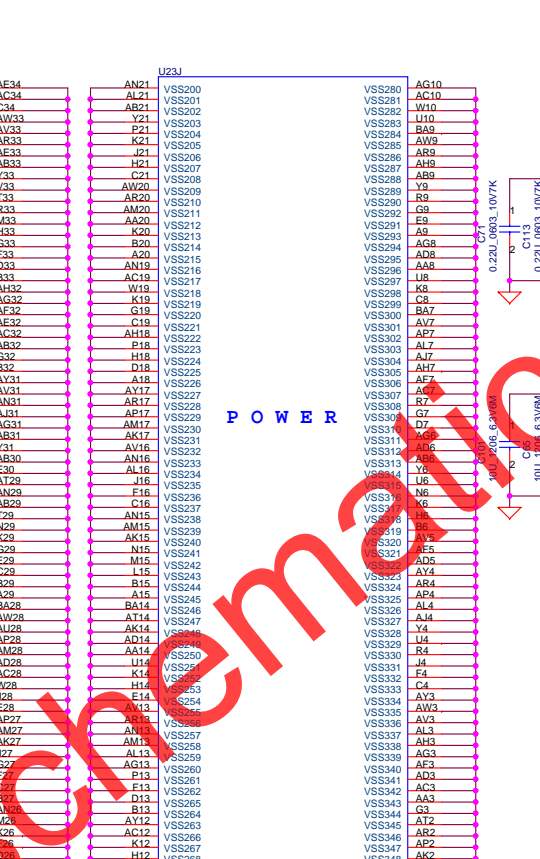
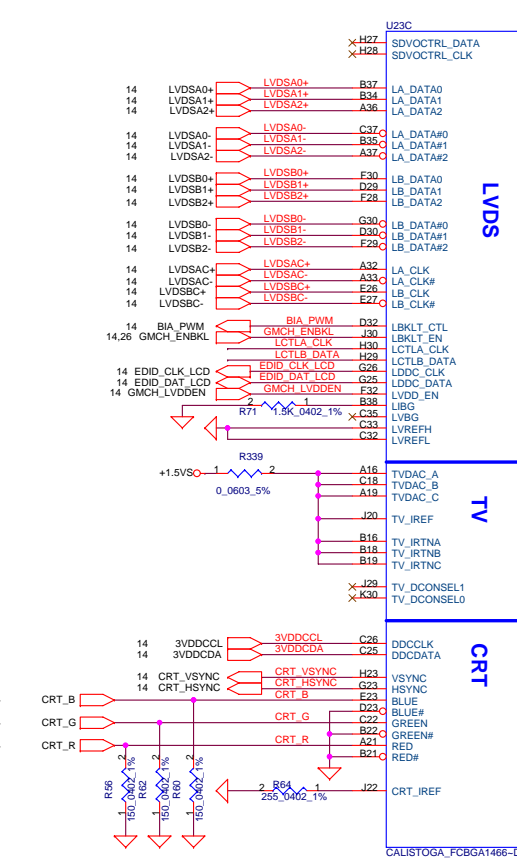
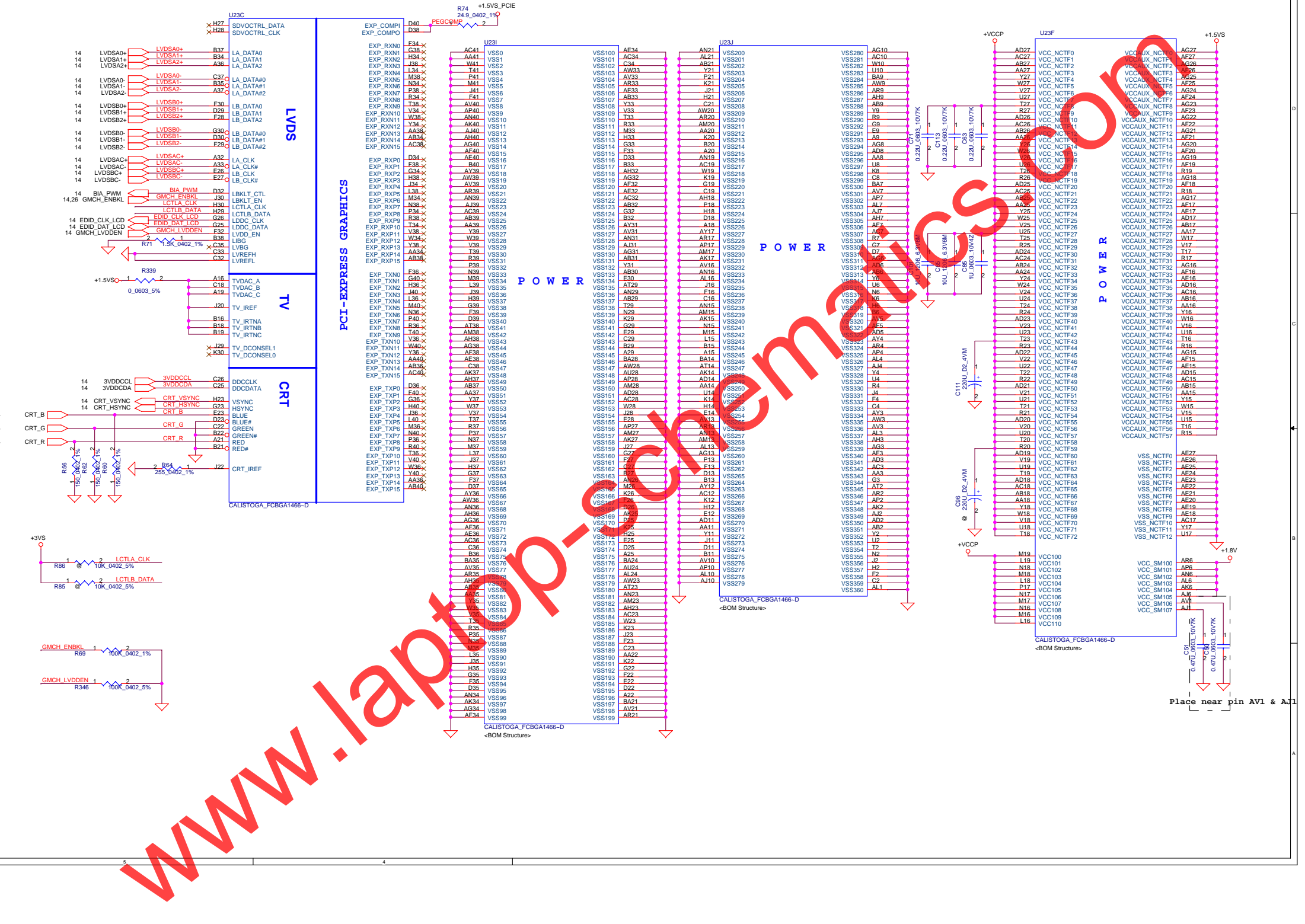


Stuff R286 & R281 for A1 Calistoga

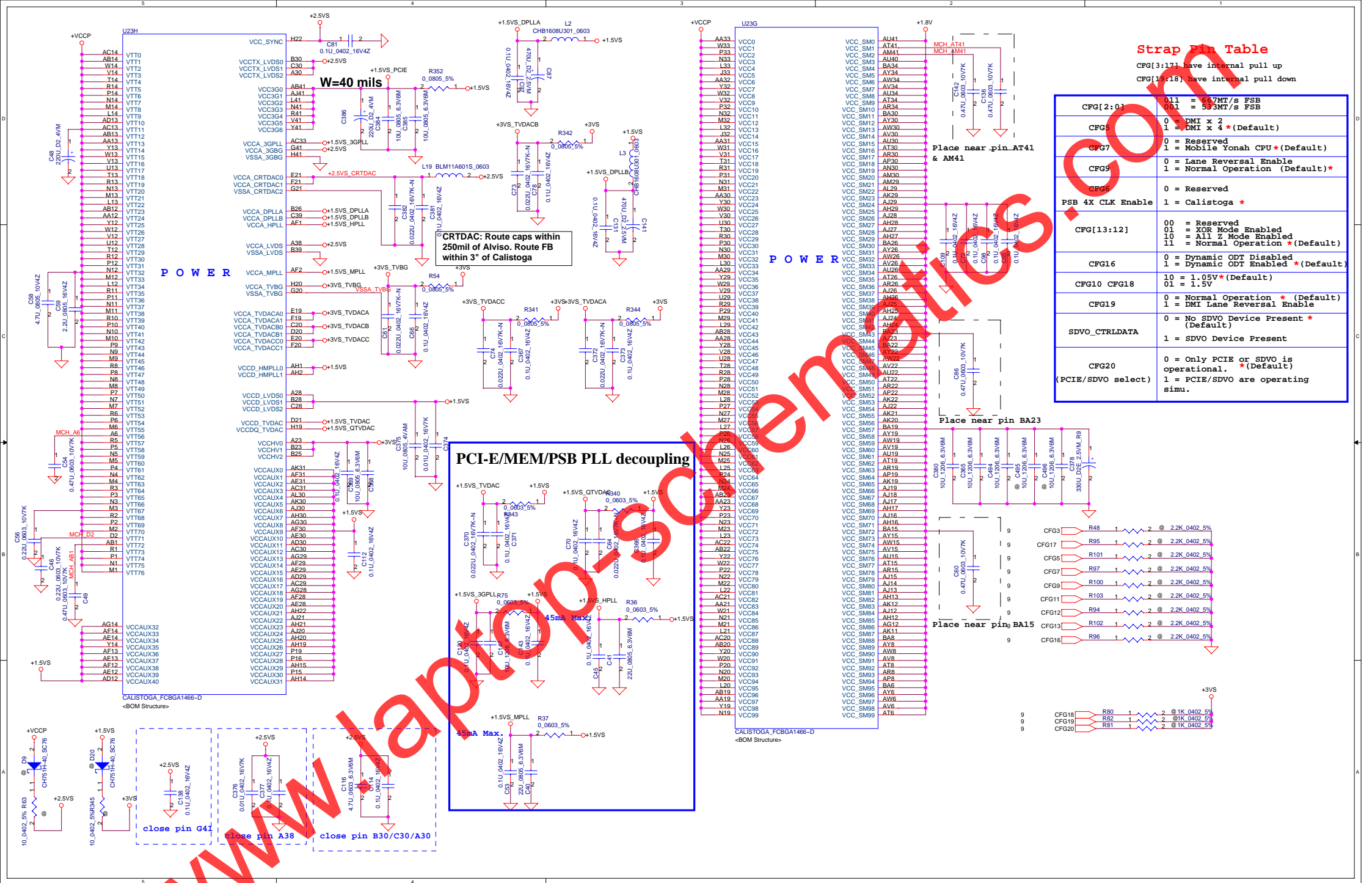




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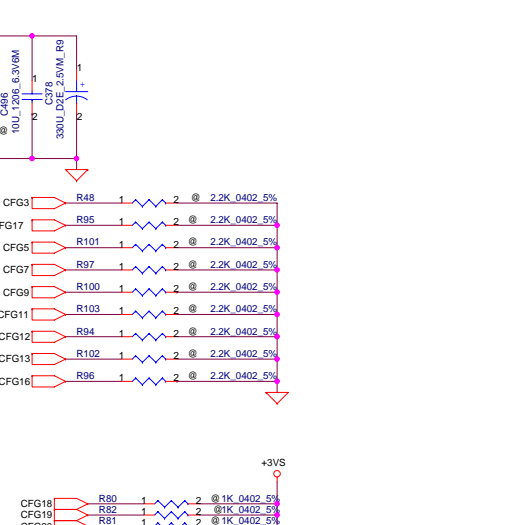
Place near pin AV1 & AV1



Strap Pin Table

CFG[3:17] have internal pull up
 CFG[19:18] have internal pull down

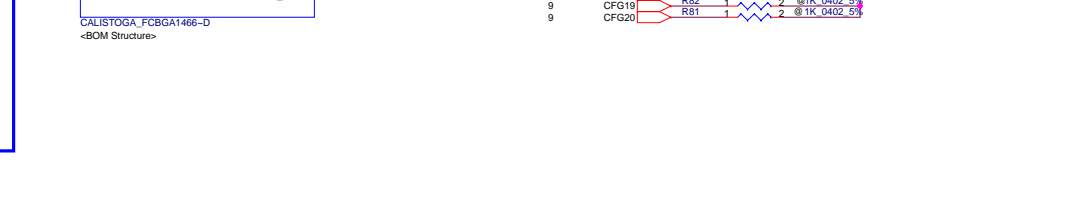
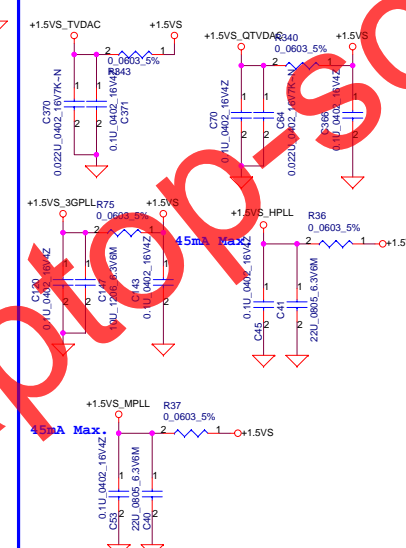
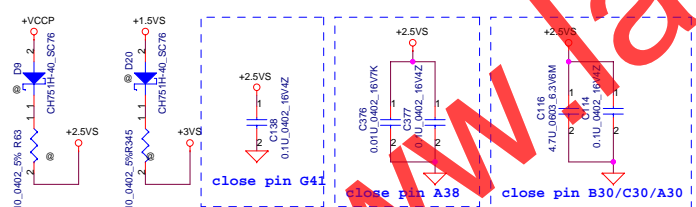
CFG[2:0]	011 = 667MT/s FSB 001 = 553MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable (Default)
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational *(Default) 1 = PCIe/SDVO are operating simu.



POWER

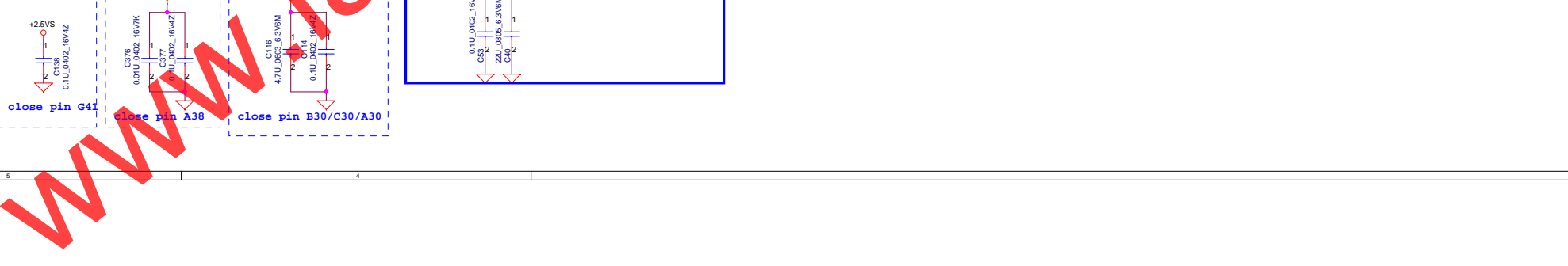
POWER

PCI-E/MEM/PSB PLL decoupling

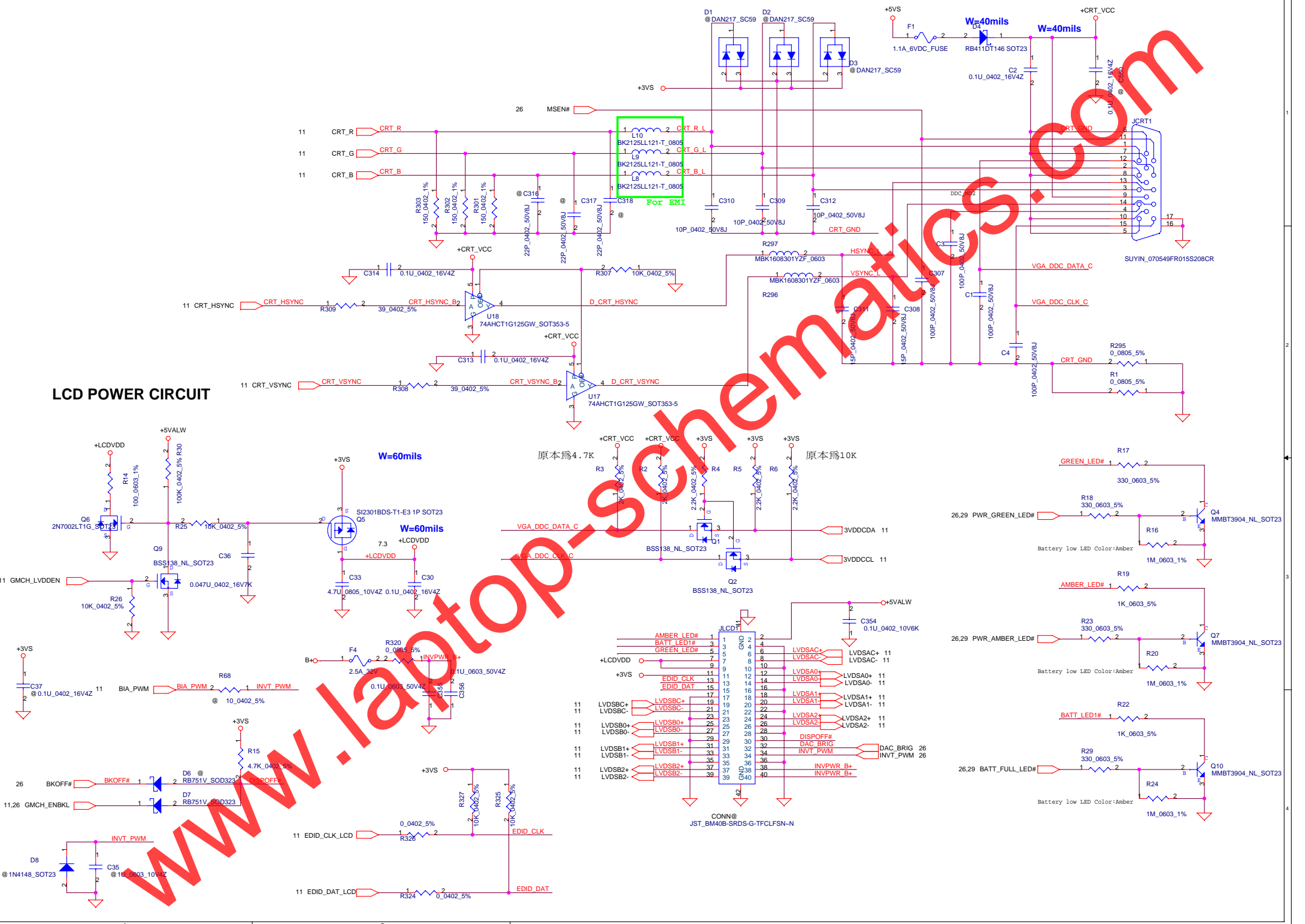


CALISTOGA_FCBGA1466-D
 <BOM Structures>

CALISTOGA_FCBGA1466-D
 <BOM Structures>

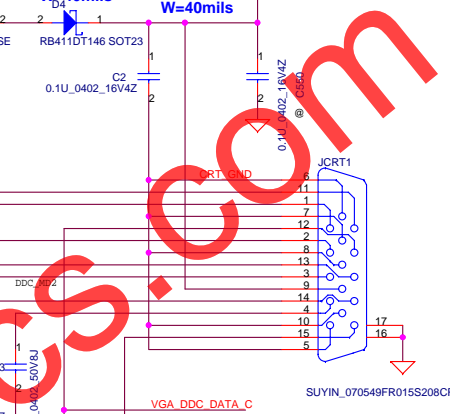


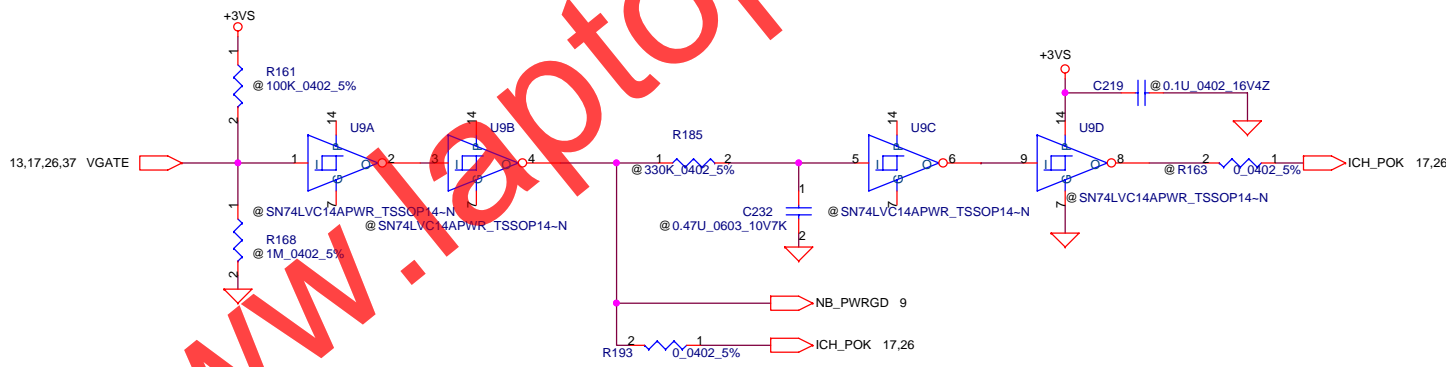
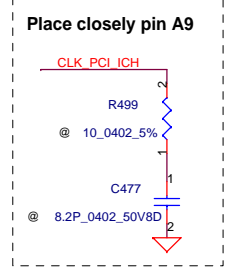
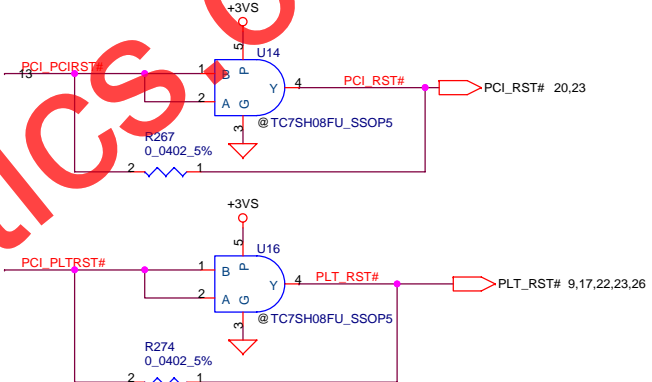
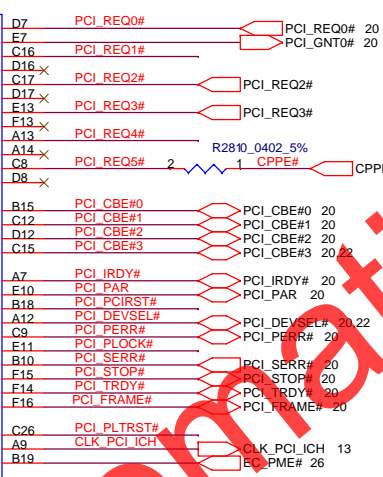
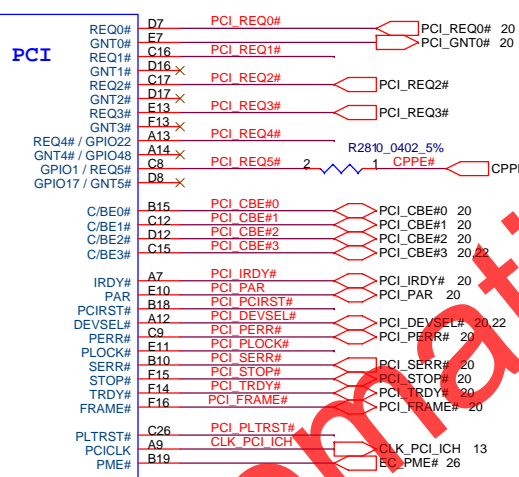
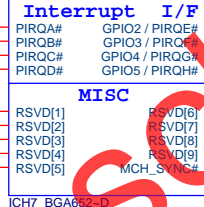
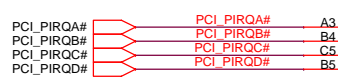
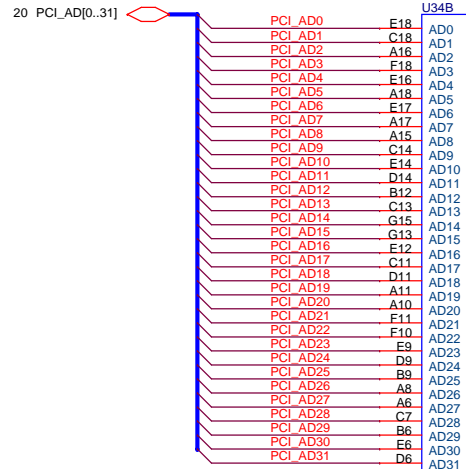
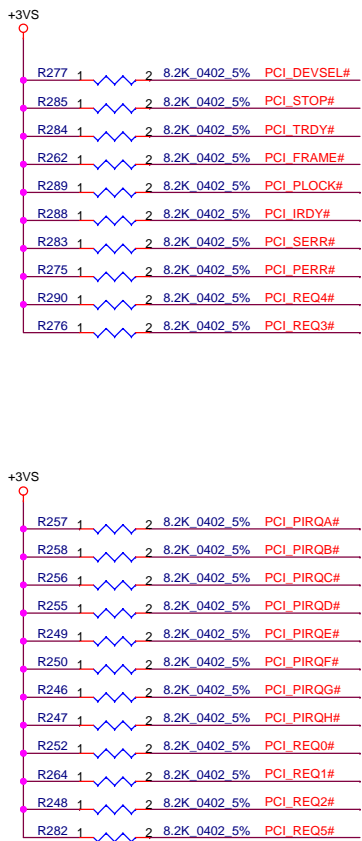
LCD POWER CIRCUIT

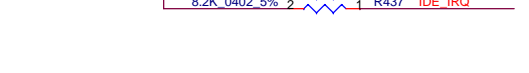
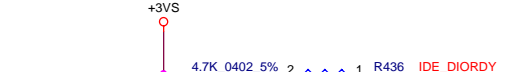
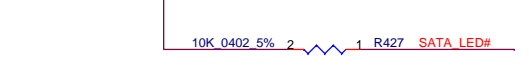
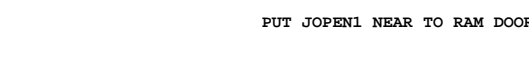
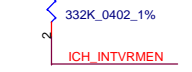
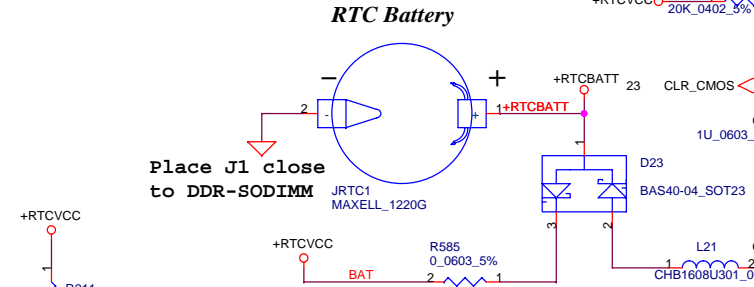
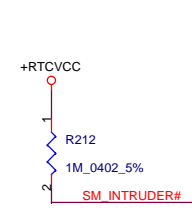
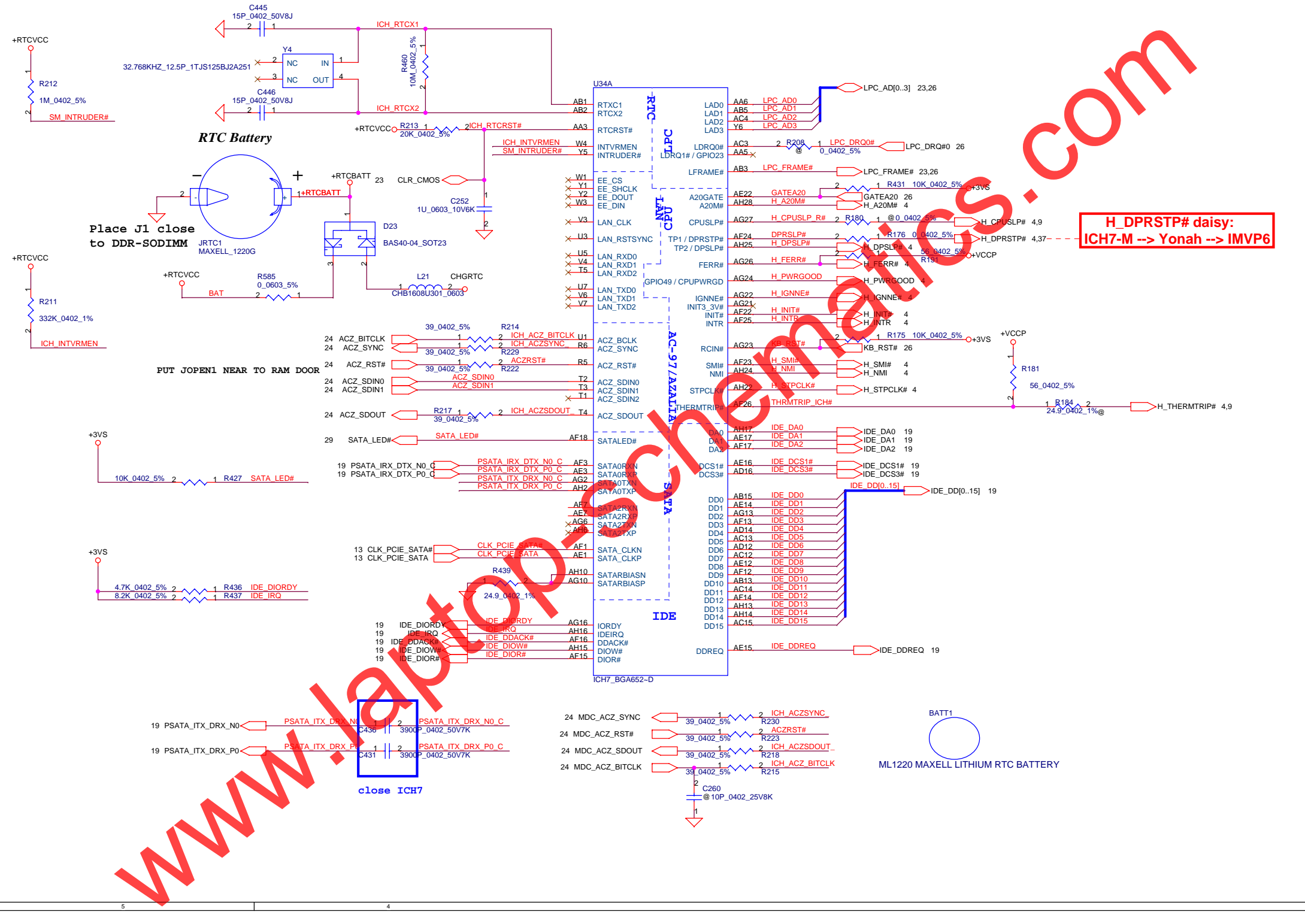


原本為4.7K
原本為10K

CONN@
JST_BM40B-SRDS-G-TFCLFSN-N

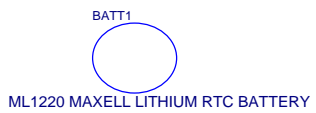




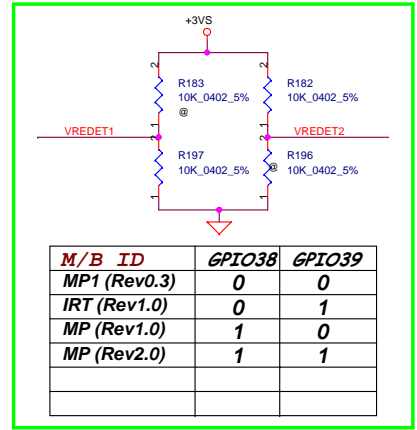
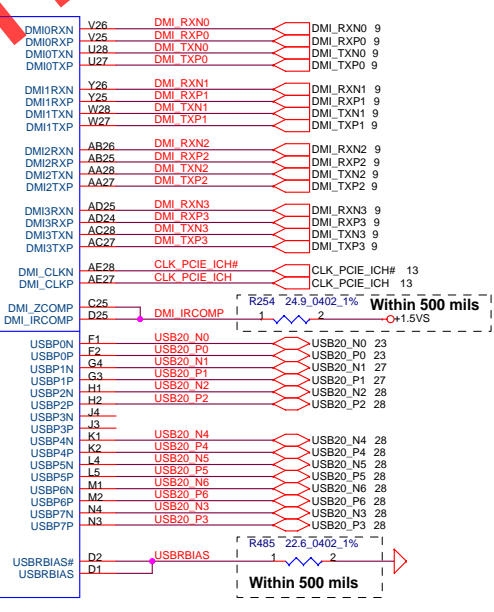
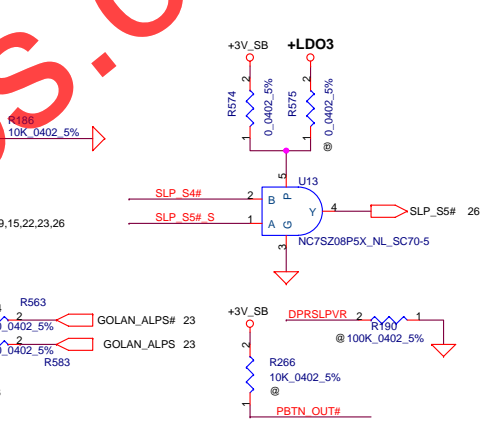
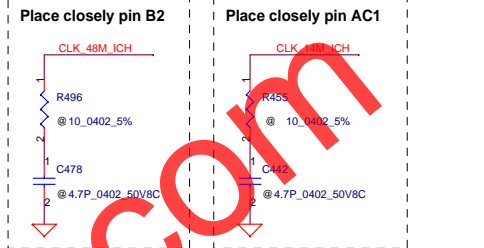
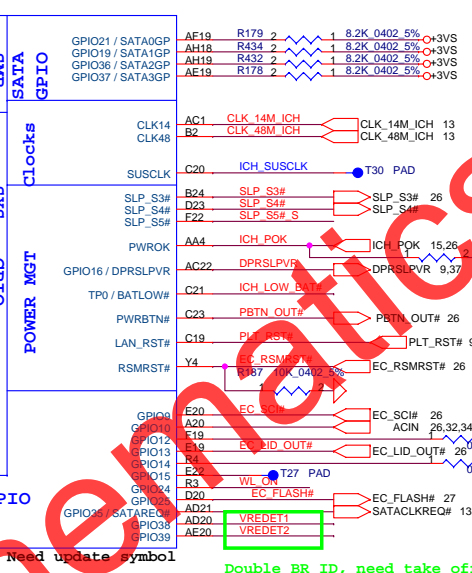
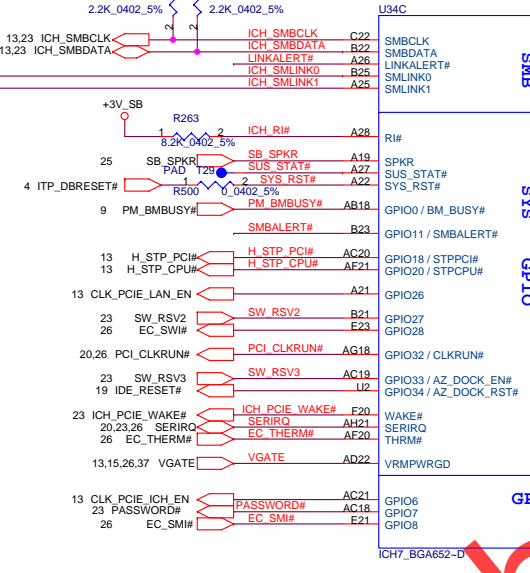
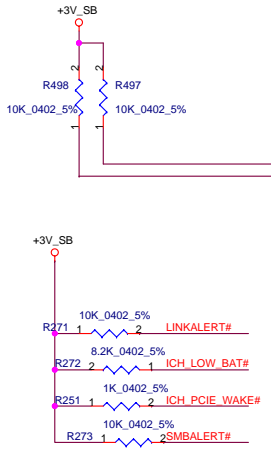
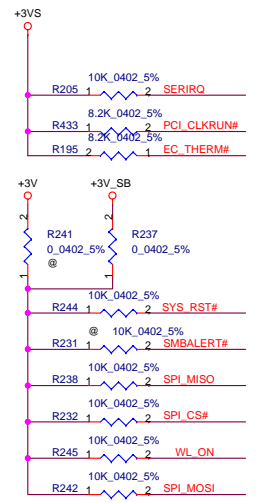


**H_DPRSTP# daisy:
 ICH7-M --> Yonah --> IMVP6**

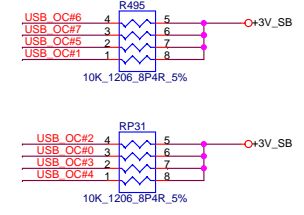
close ICH7



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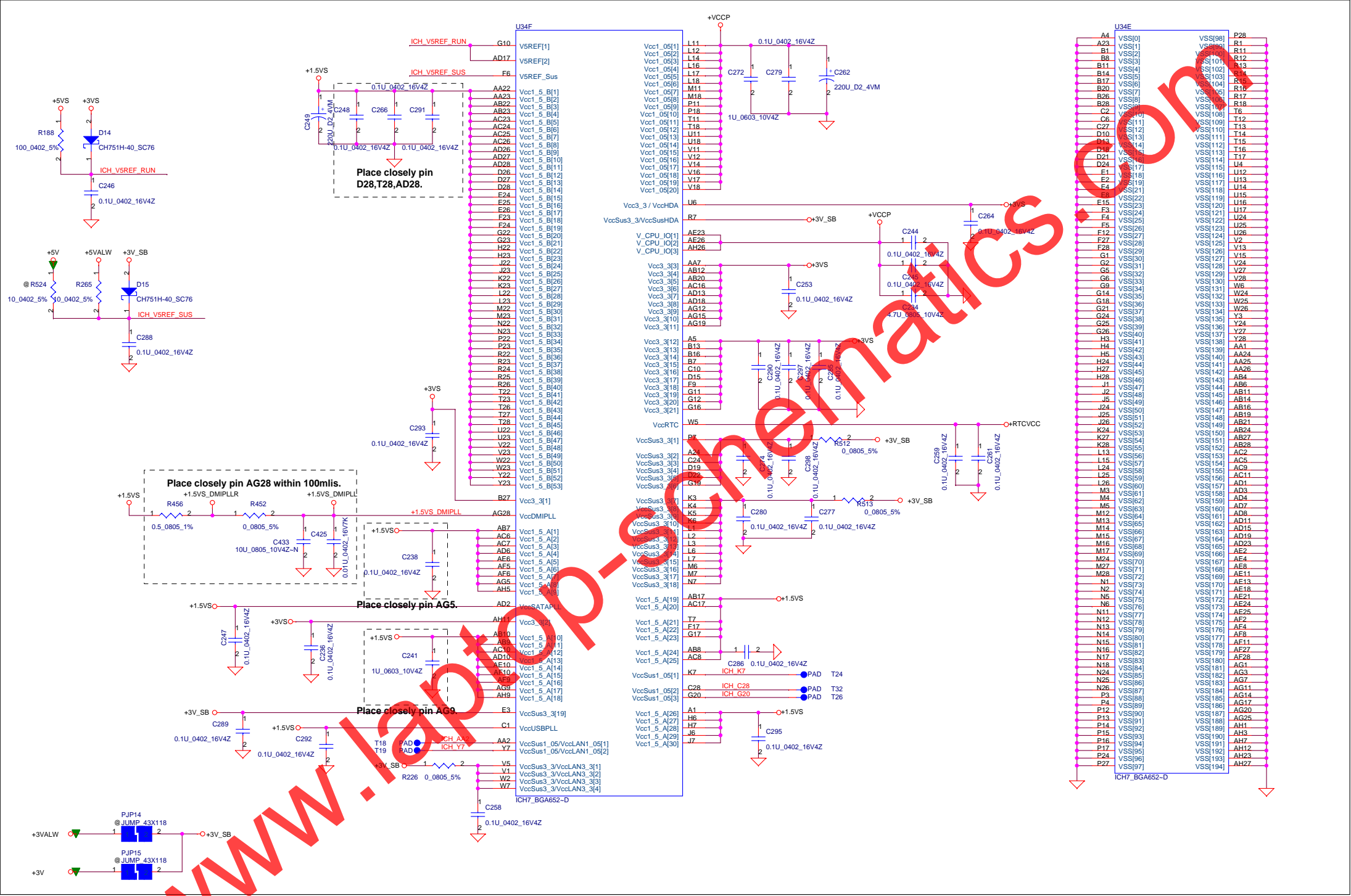


M/B ID	GPIO38	GPIO39
MP1 (Rev.0.3)	0	0
IRT (Rev1.0)	0	1
MP (Rev1.0)	1	0
MP (Rev2.0)	1	1

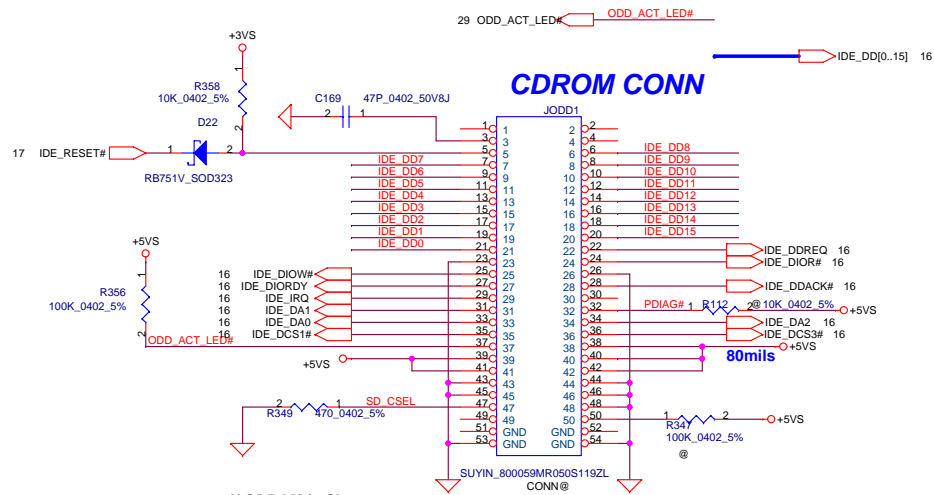


www.laptopcomponents.com

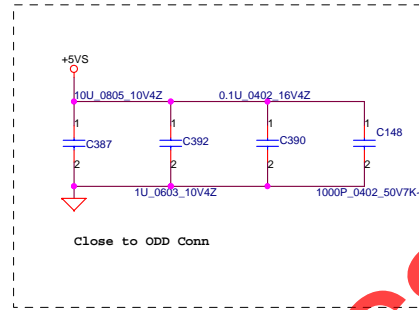
Need update symbol
Double BR ID, need take off



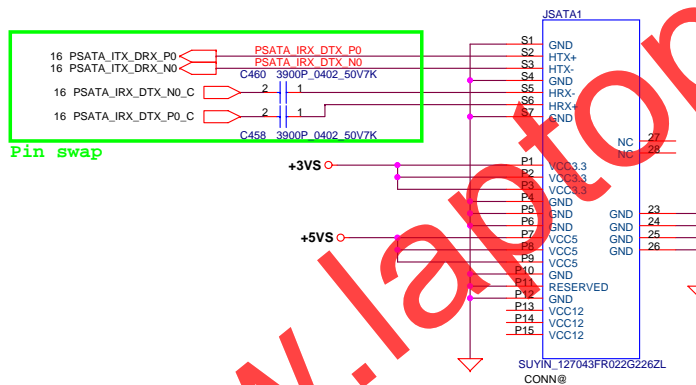
www.geminaelectronics.com



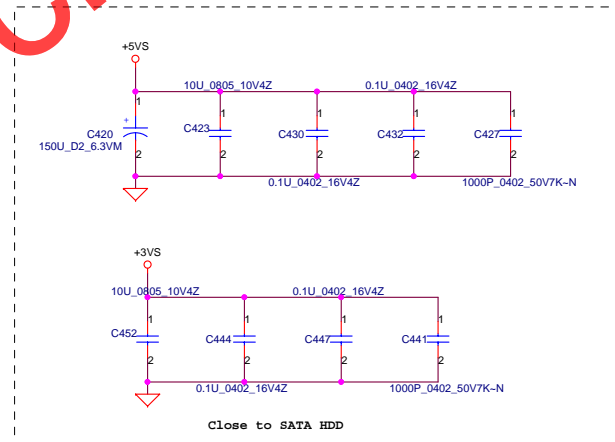
If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low



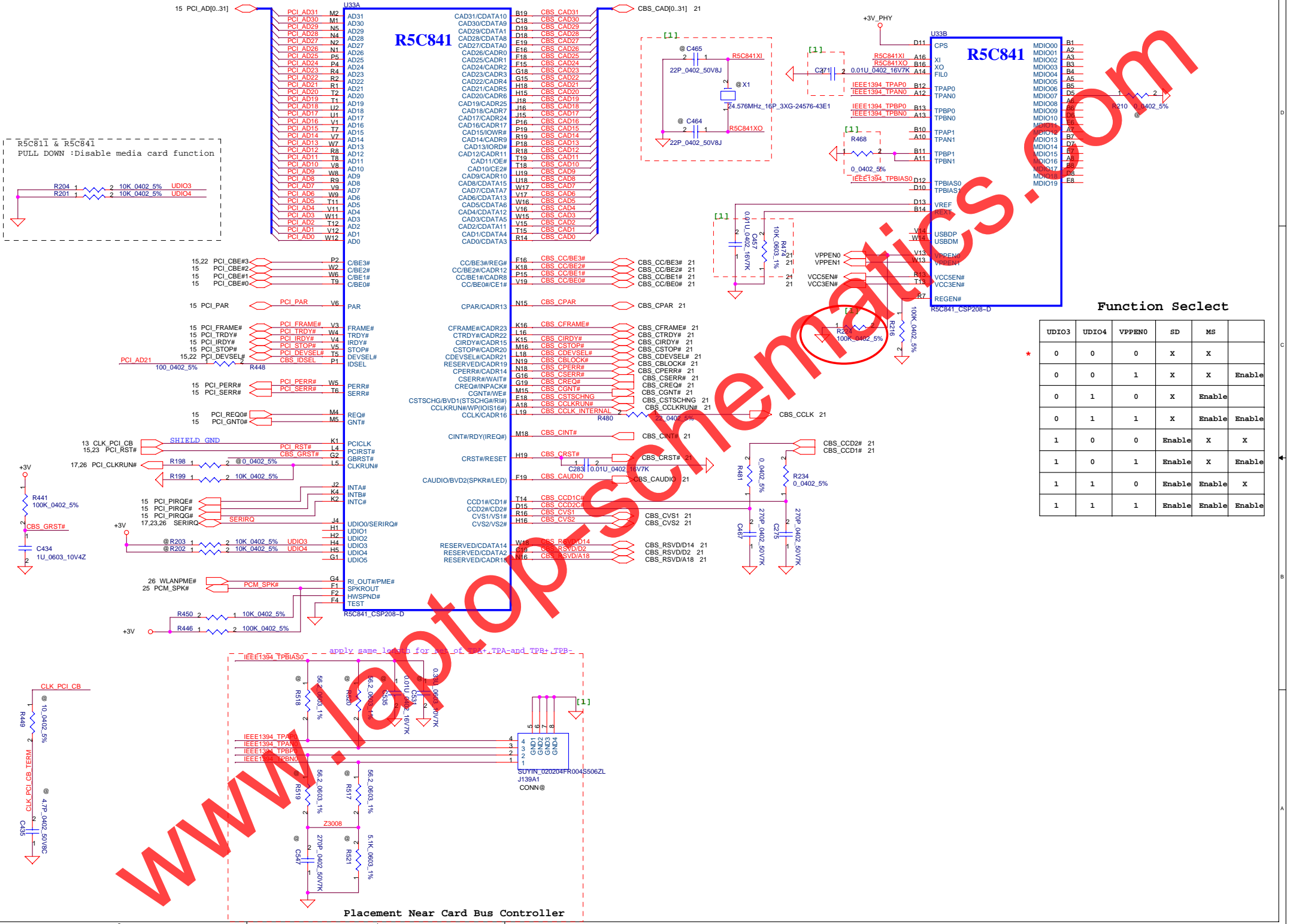
SATA HDD CONN

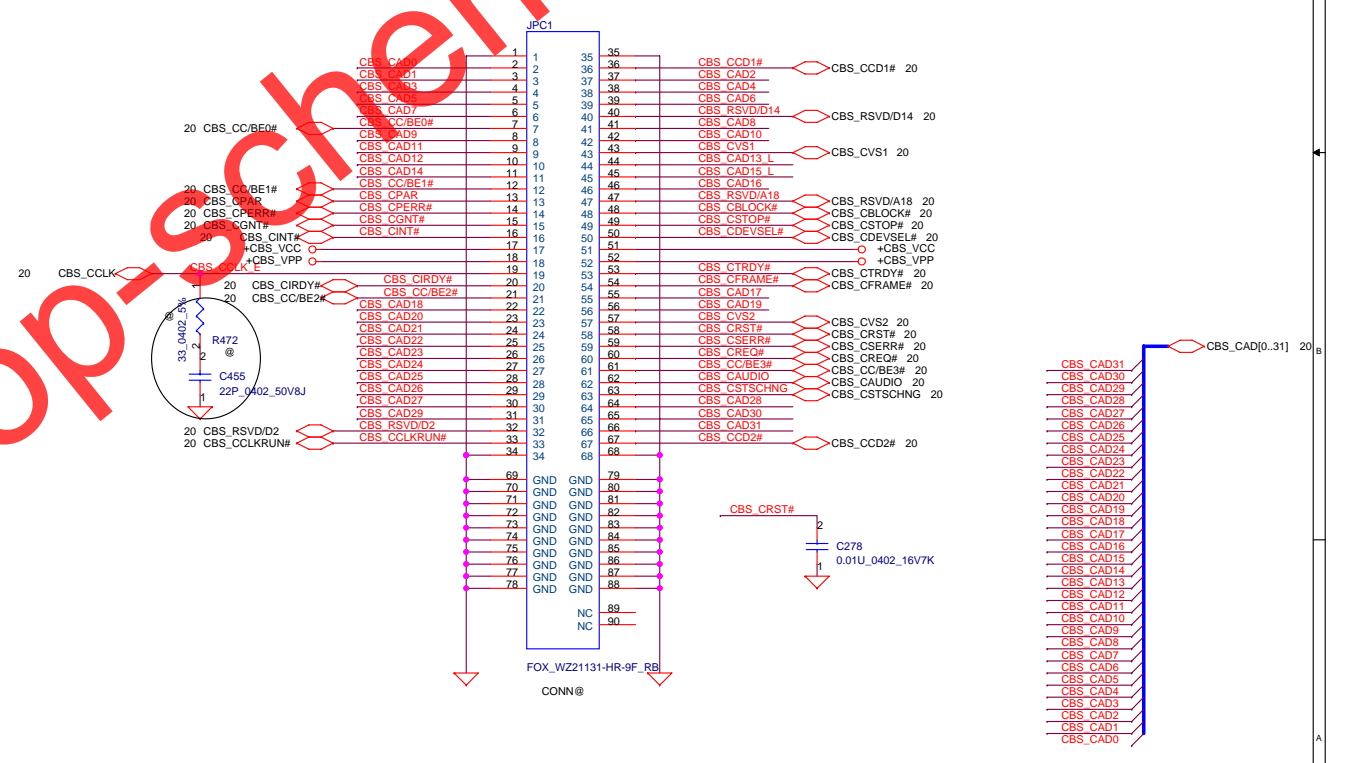
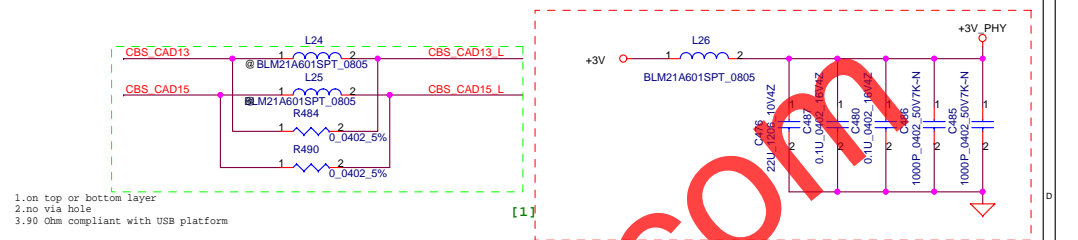
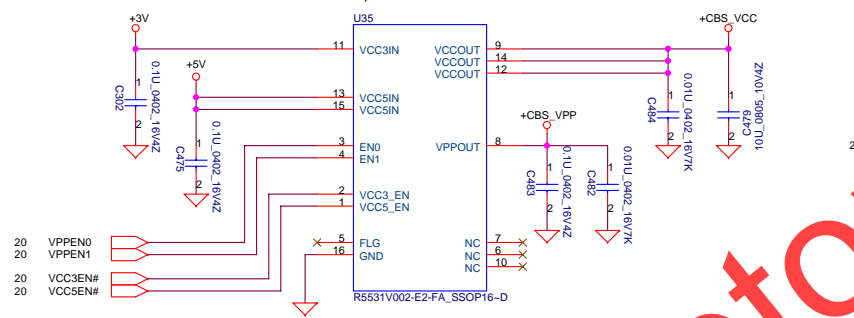
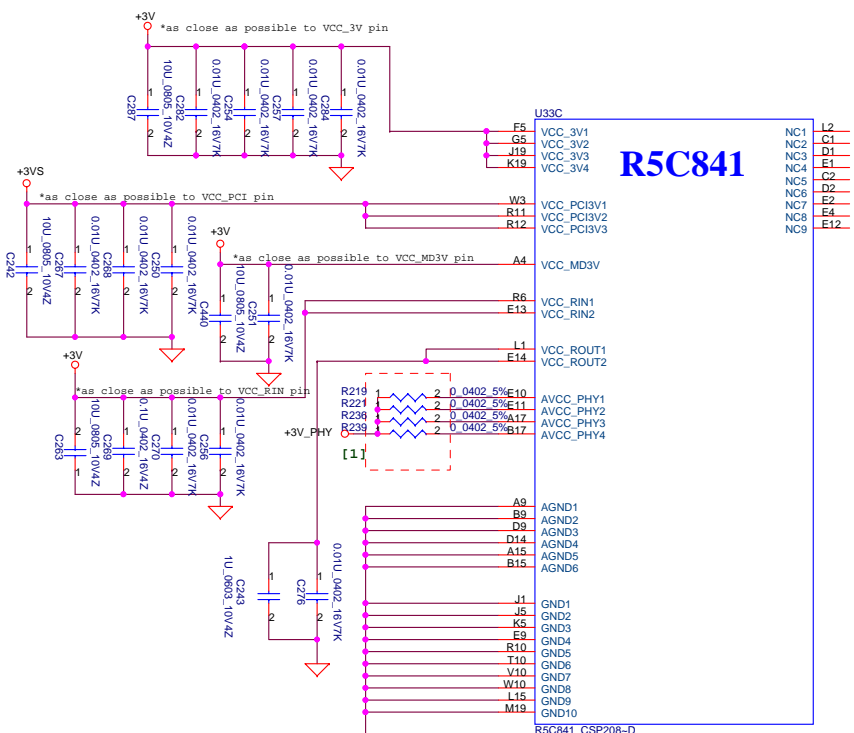


Pin swap

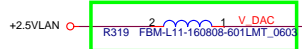


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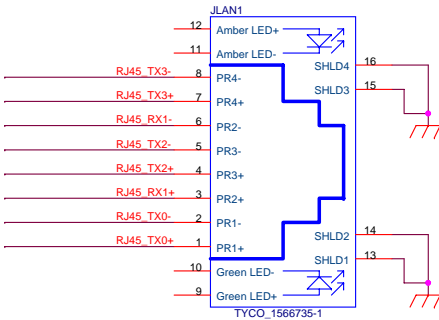
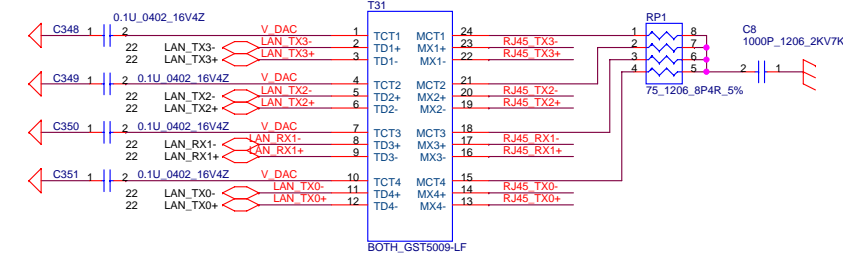




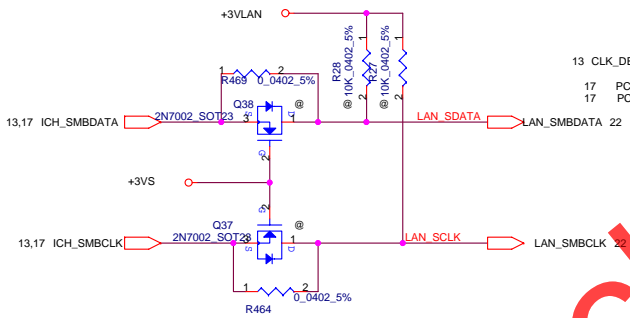
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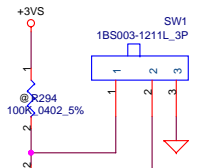
1. ES2 by rework form 0805 to 0603
2. Part name will modify in next phase



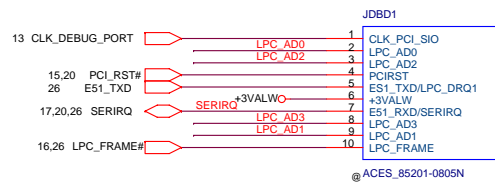
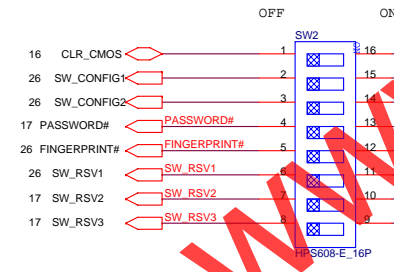
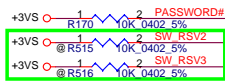
Layout Note
24HST1041A-3 pls close to conn.



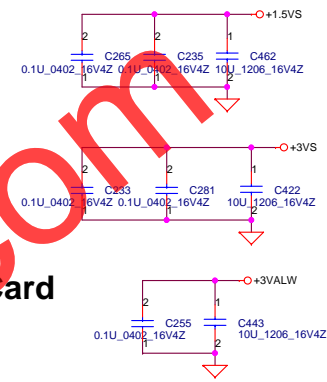
Wireless_BTN
Killer switch



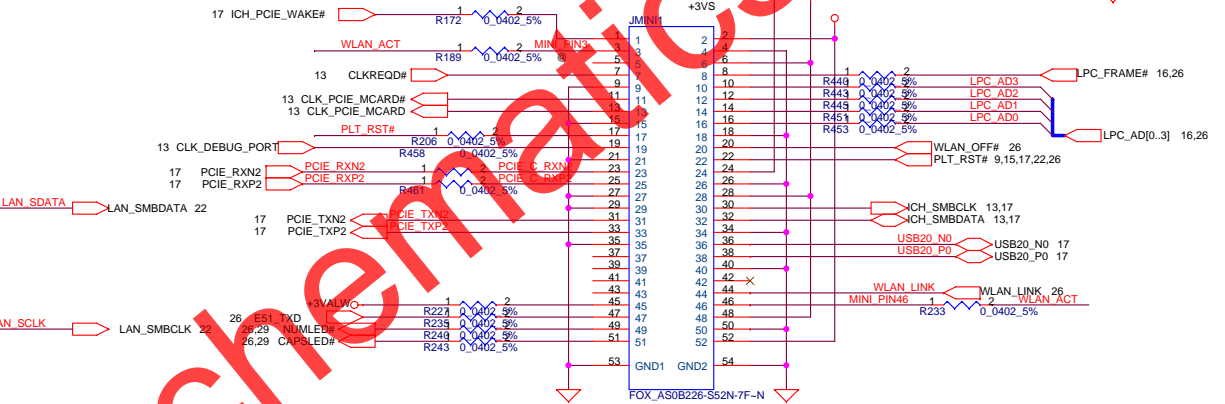
All 49.9 ohm + 0.1 uF termination components close to BCM5751M



For DEBUG

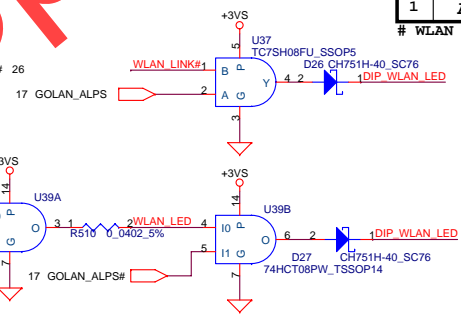


Mini-Express Card

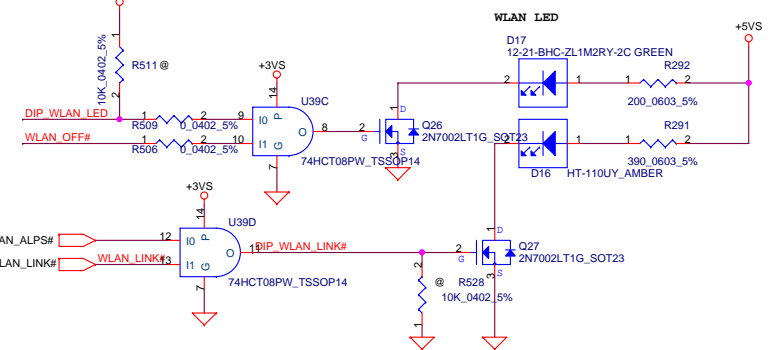


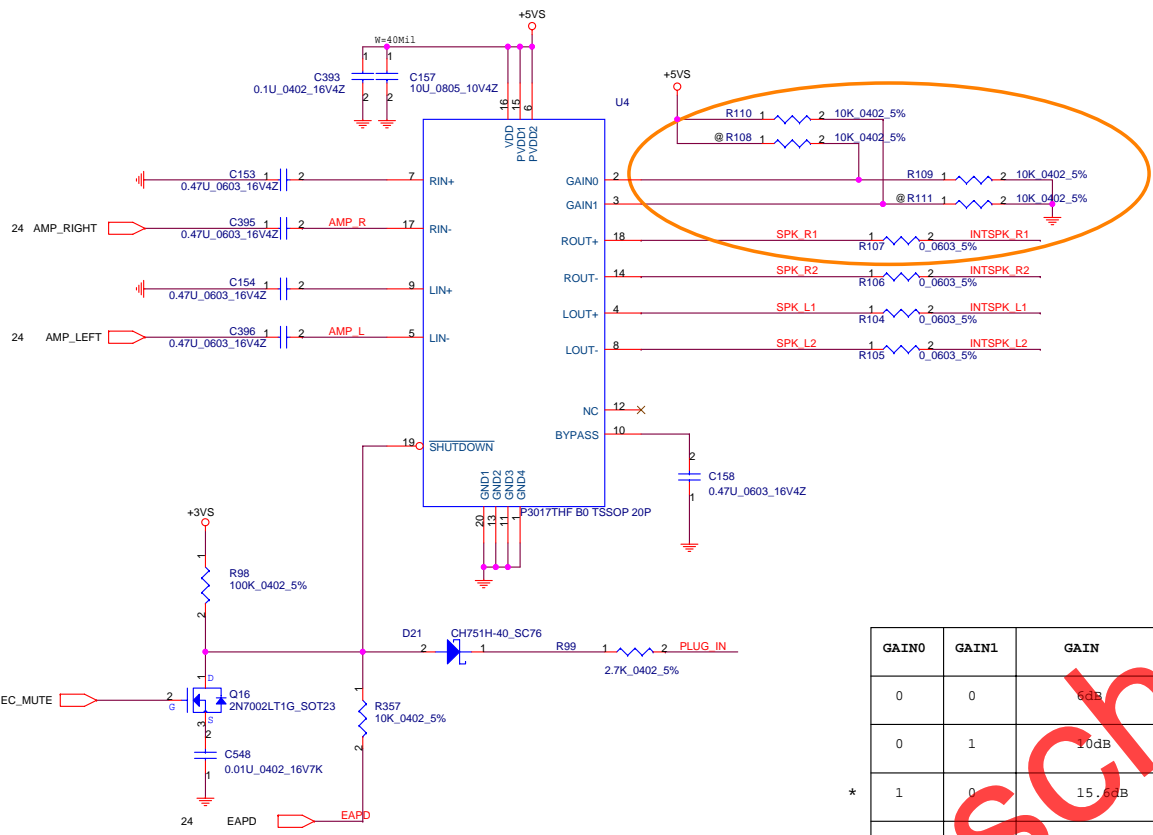
GOLAN_ALPS#	
0	GOLAN
1	ALPS

WLAN detect by BIOS and program GOLAN_ALPS# to control WLAN LED

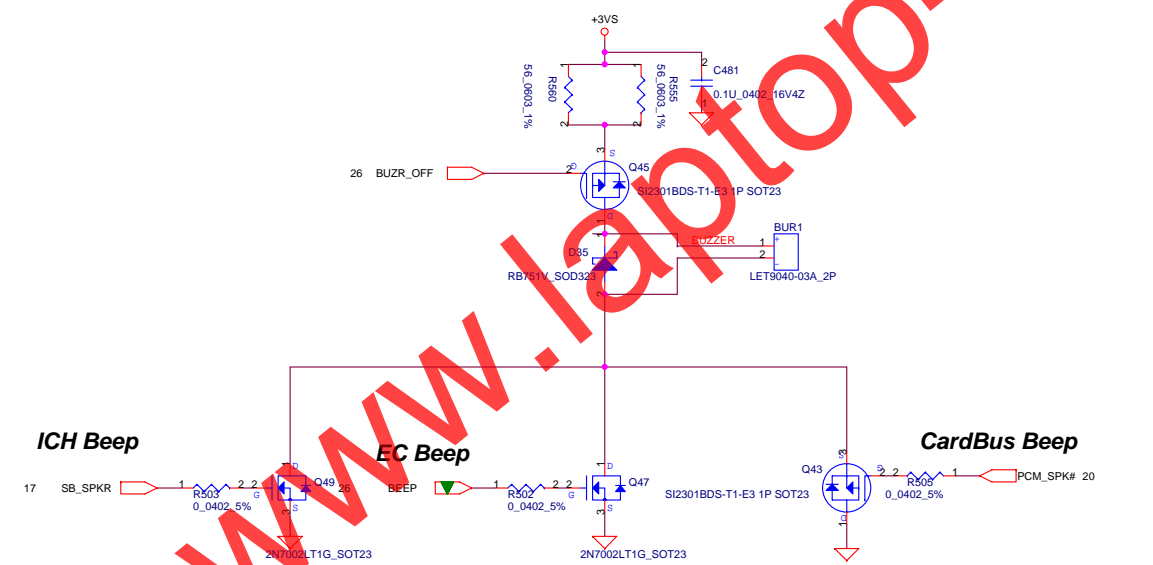


D1 Pin3 Open PAST & MASK layer

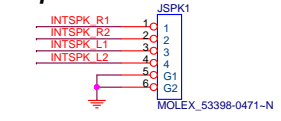




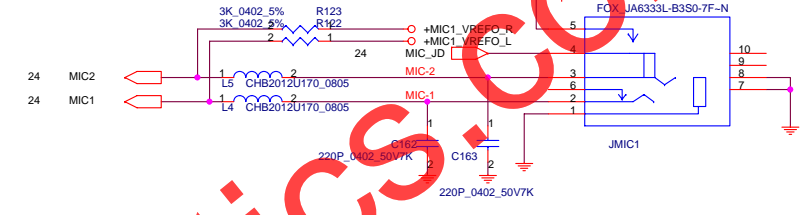
Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off



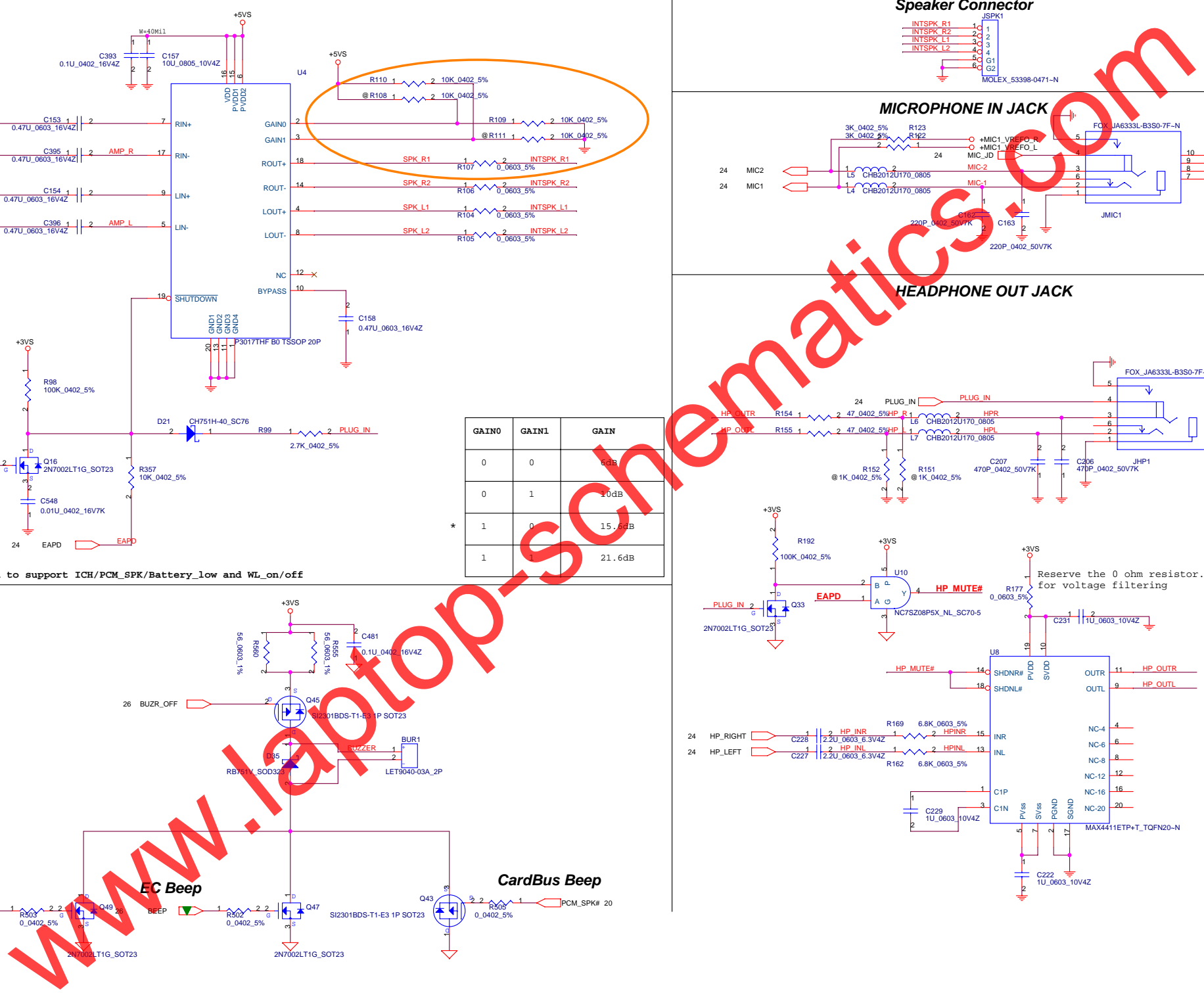
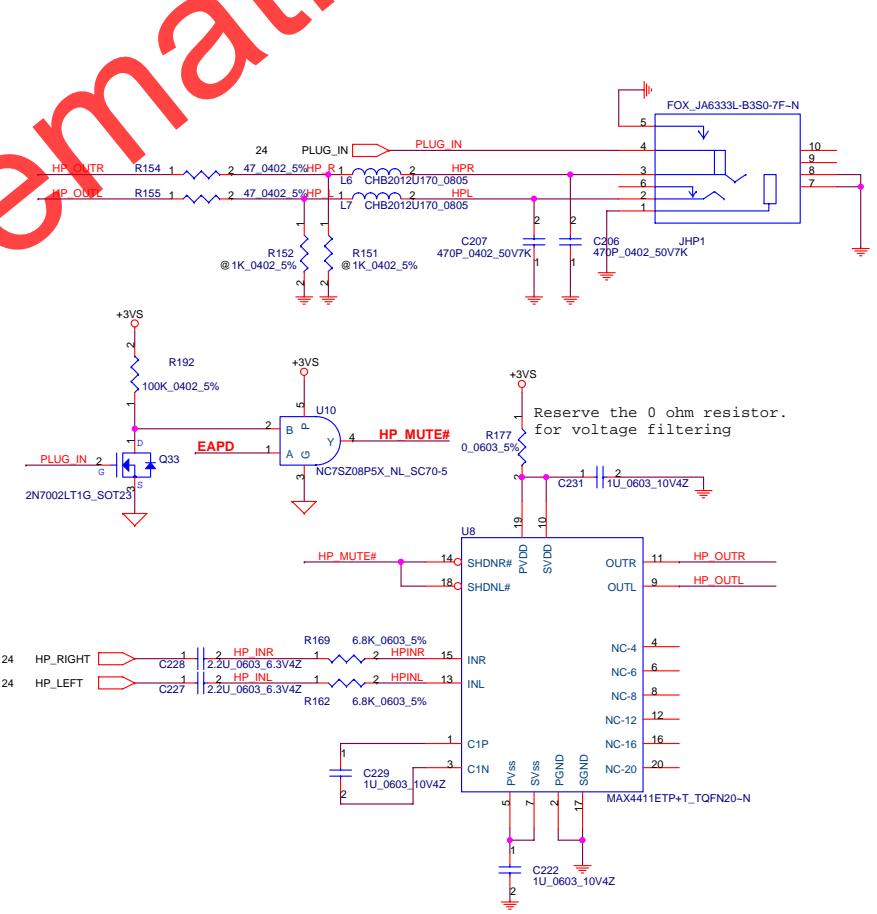
Speaker Connector

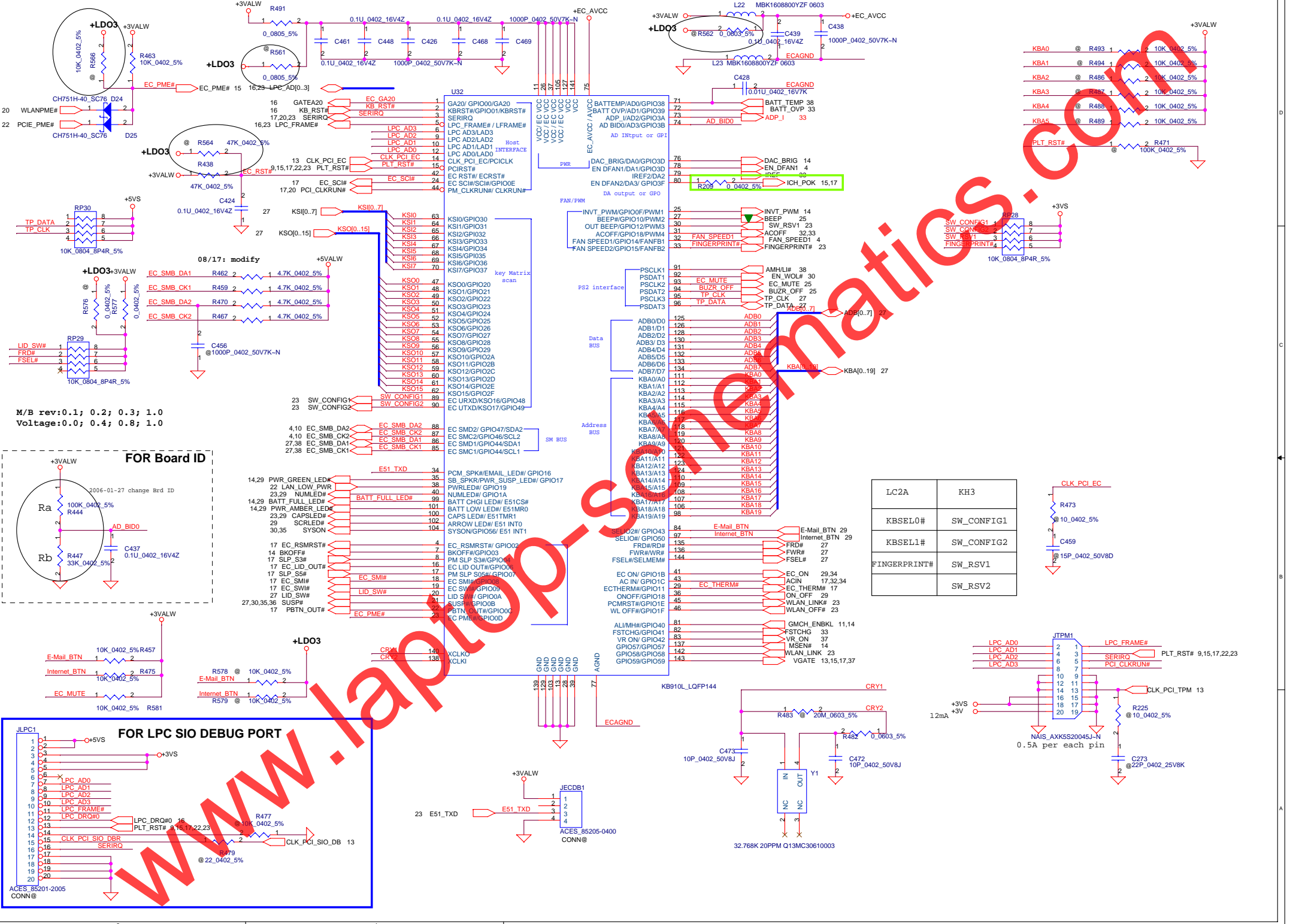


MICROPHONE IN JACK



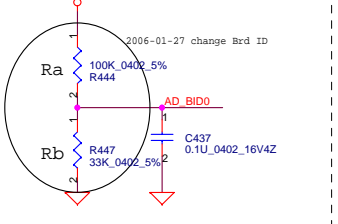
HEADPHONE OUT JACK



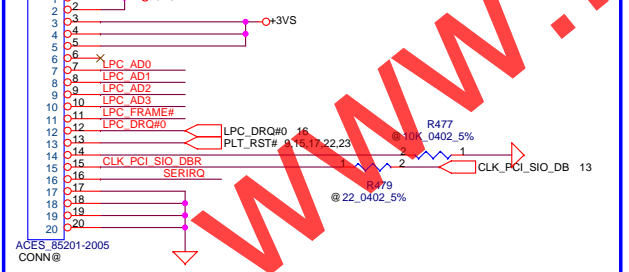


M/B rev:0.1; 0.2; 0.3; 1.0
 Voltage:0.0; 0.4; 0.8; 1.0

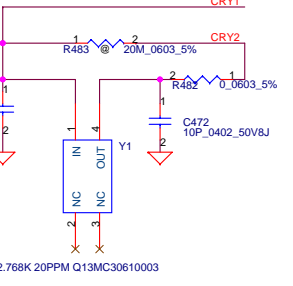
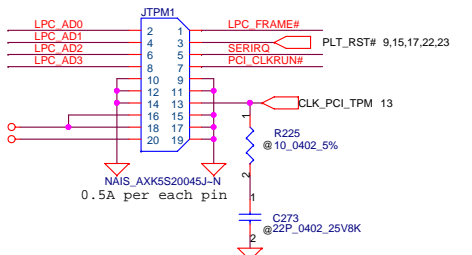
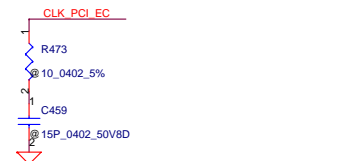
FOR Board ID



FOR LPC SIO DEBUG PORT



LC2A	KH3
KBSEL0#	SW_CONFIG1
KBSEL1#	SW_CONFIG2
FINGERPRINT#	SW_RS1
	SW_RS2



- 4,10 EC_SMB_DA2
- 4,10 EC_SMB_CK2
- 27,38 EC_SMB_DA1
- 27,38 EC_SMB_CK1
- EC SMB DA2
- EC SMB CK2
- EC SMB DA1
- EC SMB CK1

- 14,29 PWR_GREEN_LED#
- 22 LAN_LOW_PWR
- 23,29 NUMLED#
- 14,29 BATT_FULL_LED#
- 14,29 PWR_AMBER_LED#
- 23,29 CAPSLED#
- 29 SCRDLED#
- 30,35 SYSDON
- 17 EC_RSMRST#
- 14 BKOFF#
- 17 SLP_S#
- 17 EC_LID_OUT#
- 17 SLP_S#
- 17 EC_SMI#
- 17 EC_SWI#
- 27 LID_SW#
- 27,30,35,36 SUSP#
- 17 PBTN_OUT#
- EC PME#

- 140 CRV1
- 138 CRV2
- XCLKO
- NCKI

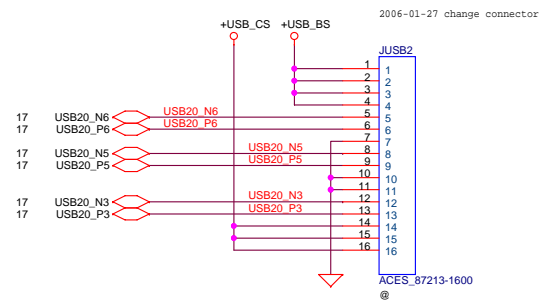
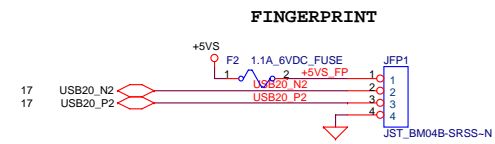
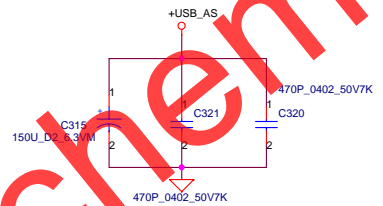
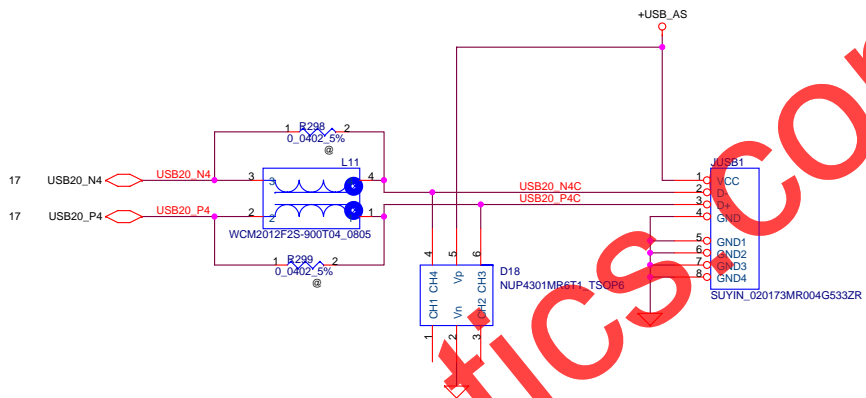
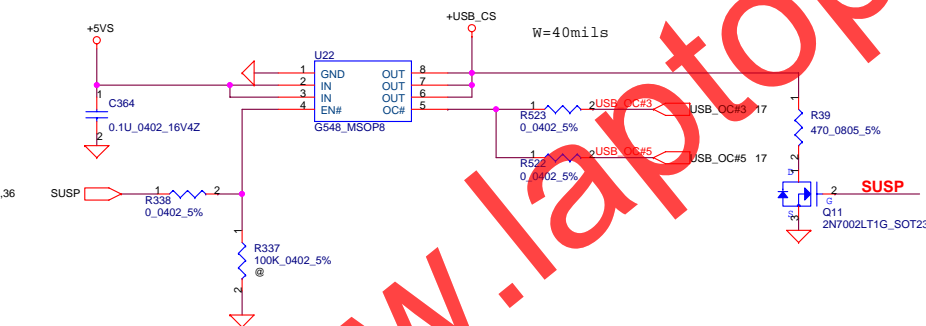
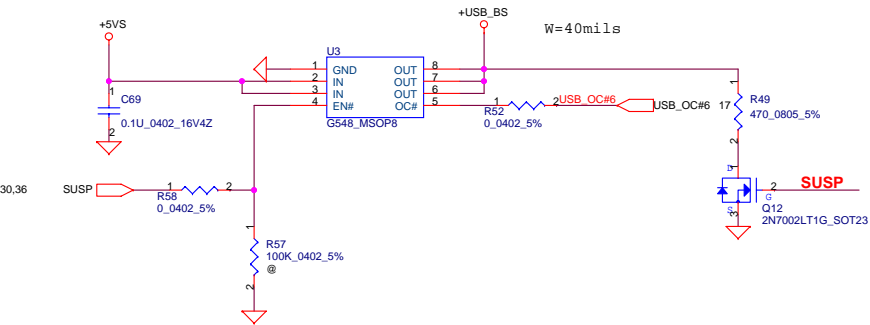
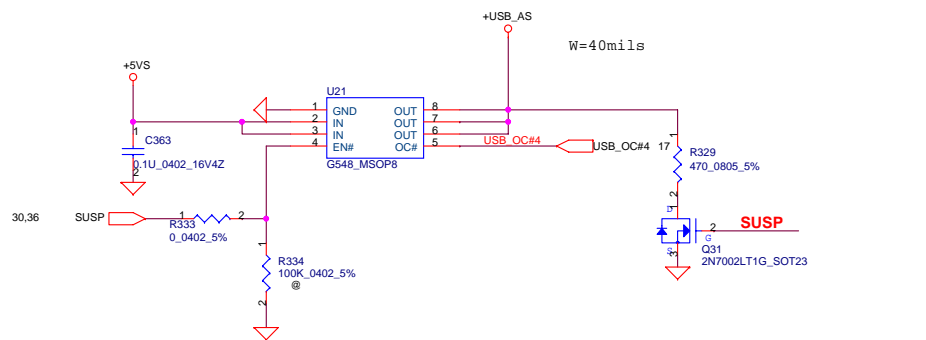
- 138 GND
- 128 GND
- 103 GND
- 28 GND
- 38 GND
- 77 AGND

- 138 GND
- 128 GND
- 103 GND
- 28 GND
- 38 GND
- 77 AGND

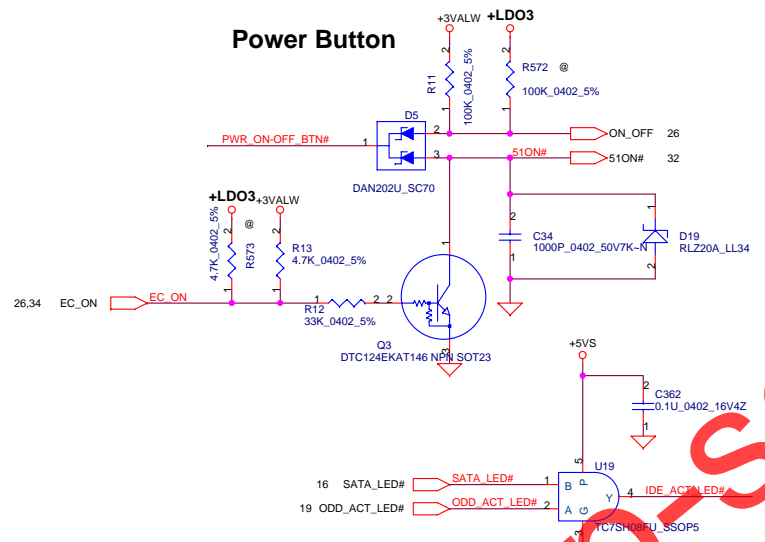
- 138 GND
- 128 GND
- 103 GND
- 28 GND
- 38 GND
- 77 AGND

- 138 GND
- 128 GND
- 103 GND
- 28 GND
- 38 GND
- 77 AGND

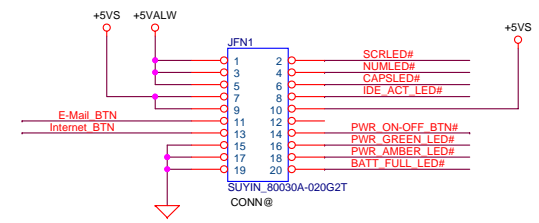
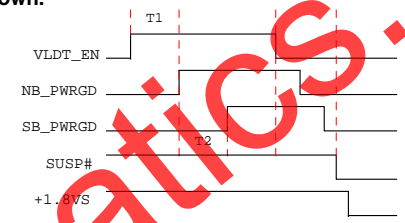
- 138 GND
- 128 GND
- 103 GND
- 28 GND
- 38 GND
- 77 AGND



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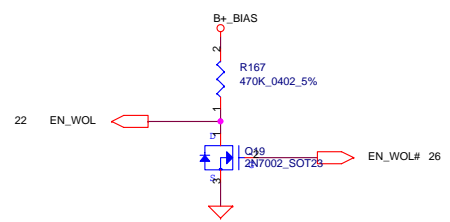
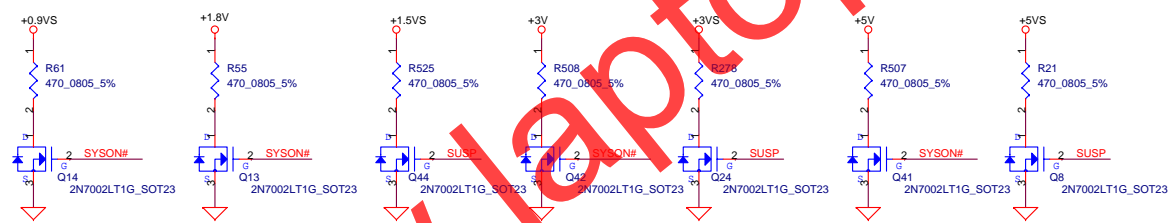
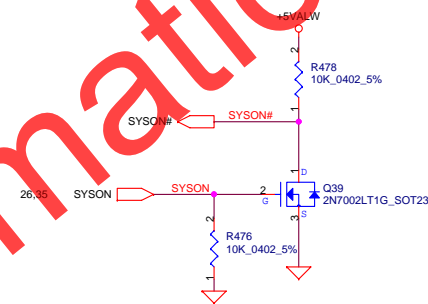
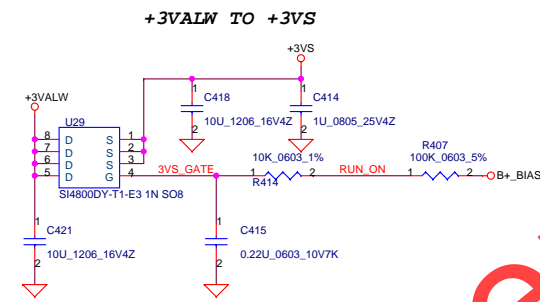
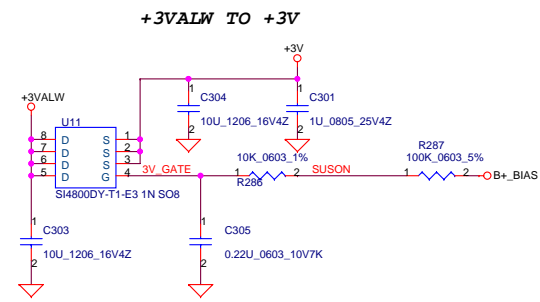
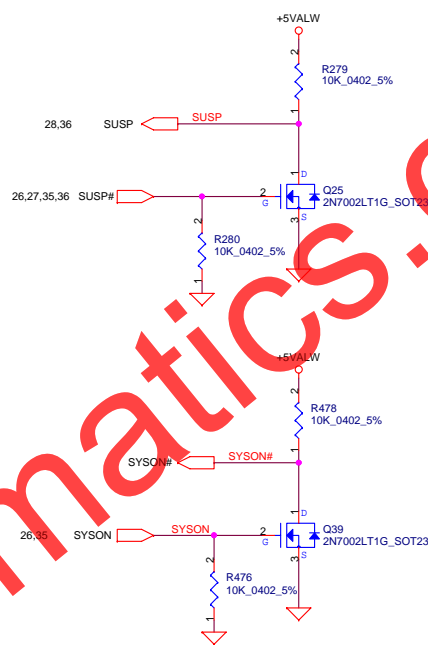
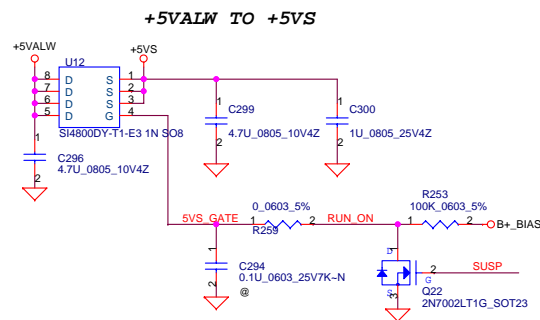
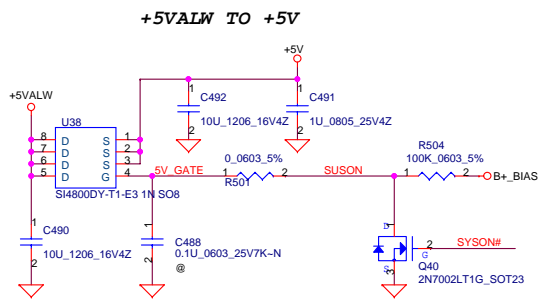
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



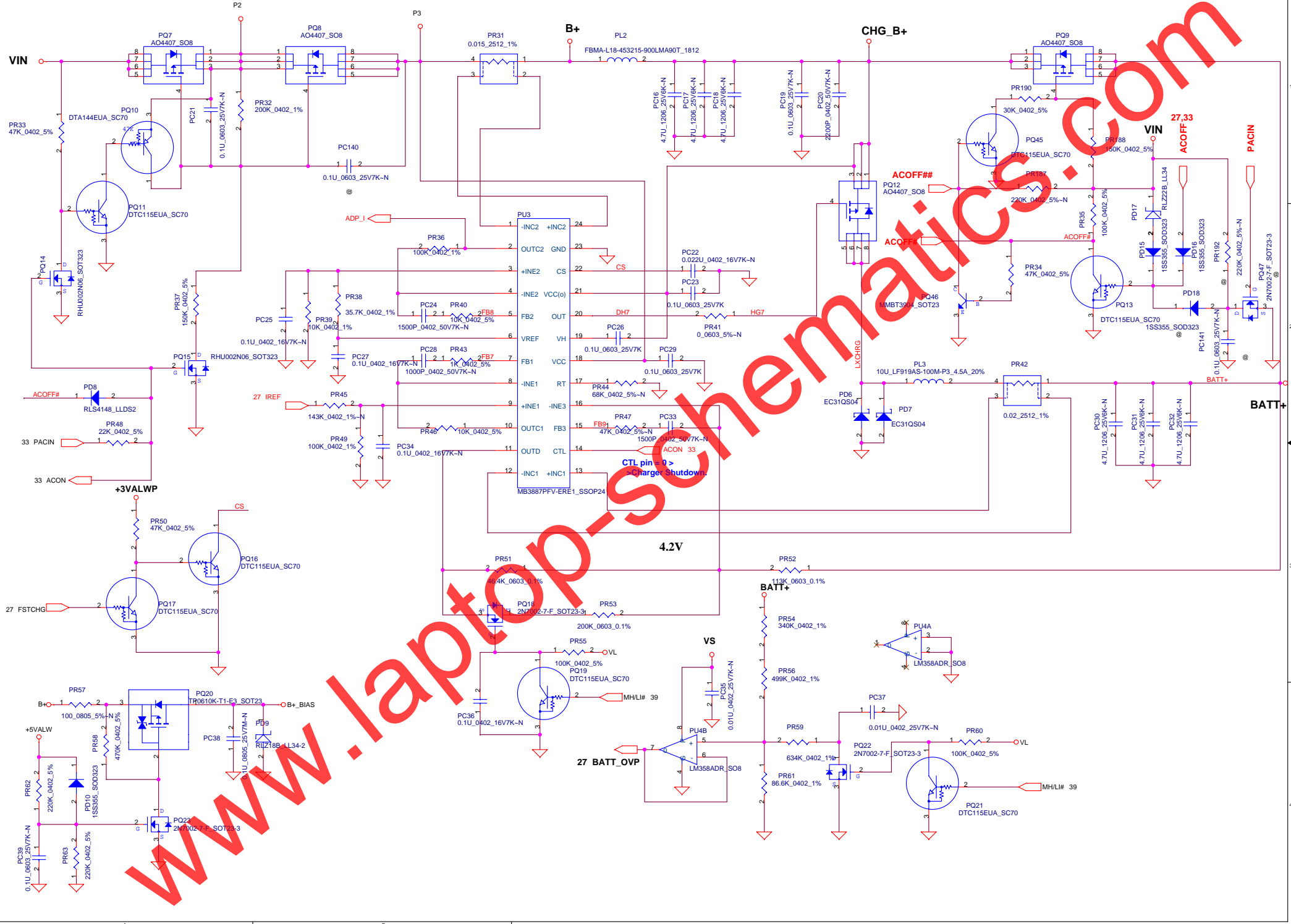
- 26 SCRLED#
- 23,26 NUMLED#
- 23,26 CAPSLED#
- 26 E-Mail_BTN
- 26 Internet_BTN
- 14,26 PWR_GREEN_LED#
- 14,26 PWR_AMBER_LED#
- 14,26 BATT_FULL_LED#

- E-Mail_BTN @ C22 100P_0402_25V8K
- Internet_BTN @ C23 100P_0402_25V8K
- SCRLED# @ C24 100P_0402_25V8K
- NUMLED# @ C25 100P_0402_25V8K
- CAPSLD# @ C32 100P_0402_25V8K
- IDE_ACT_LED# @ C26 100P_0402_25V8K
- PWR_ON-OFF_BTN# @ C27 100P_0402_25V8K
- PWR_GREEN_LED# @ C28 100P_0402_25V8K
- PWR_AMBER_LED# @ C31 100P_0402_25V8K
- BATT_FULL_LED# @ C29 100P_0402_25V8K

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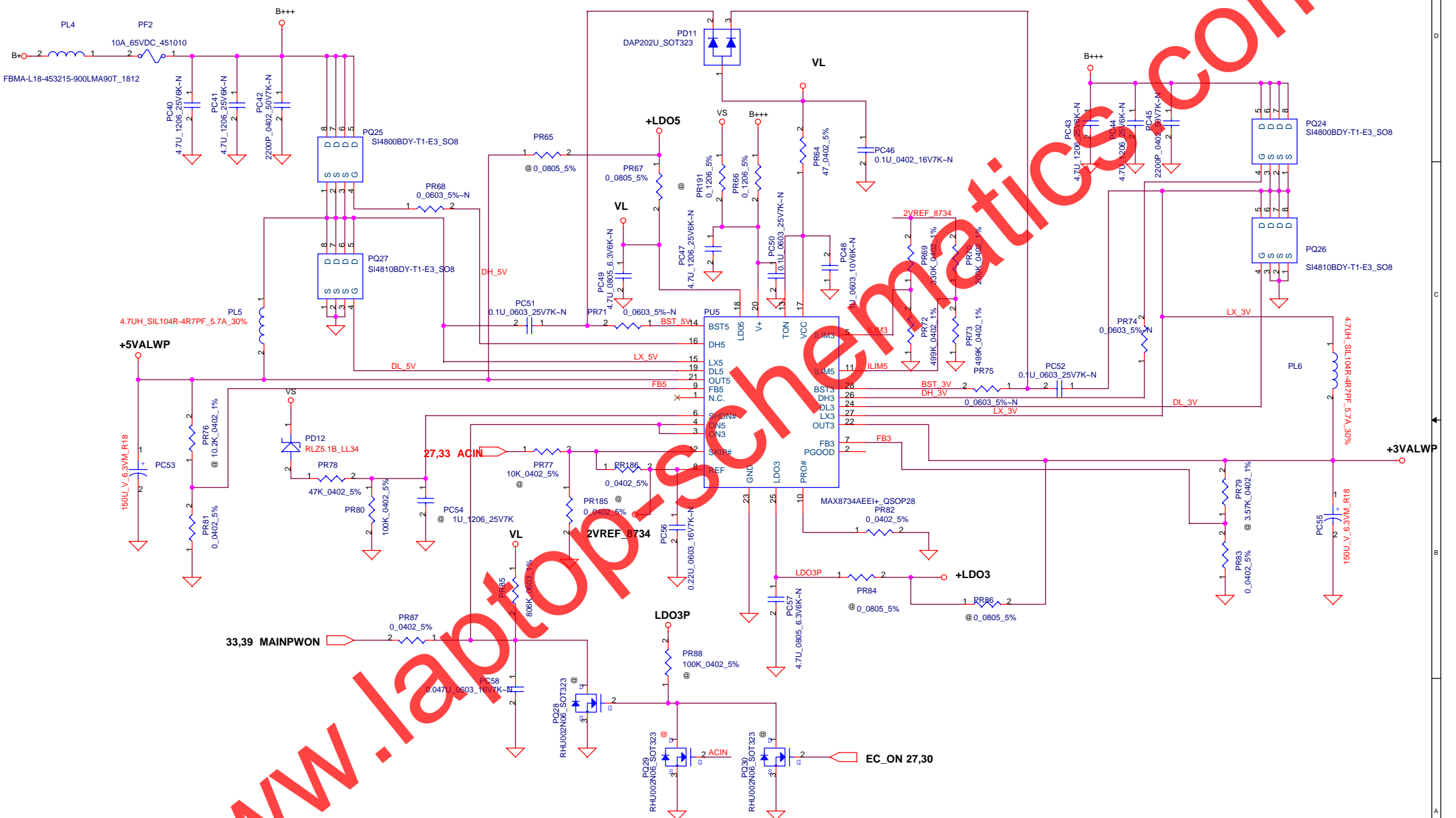


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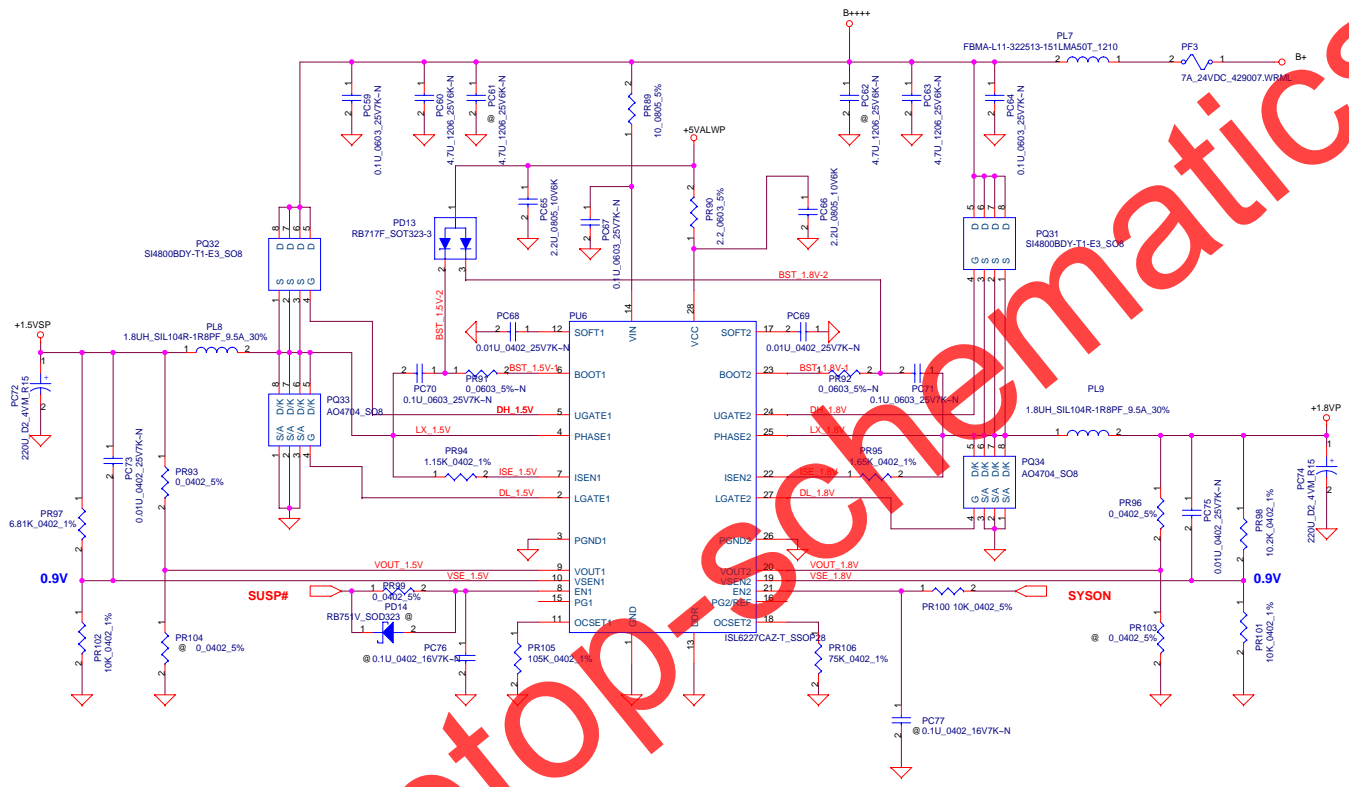
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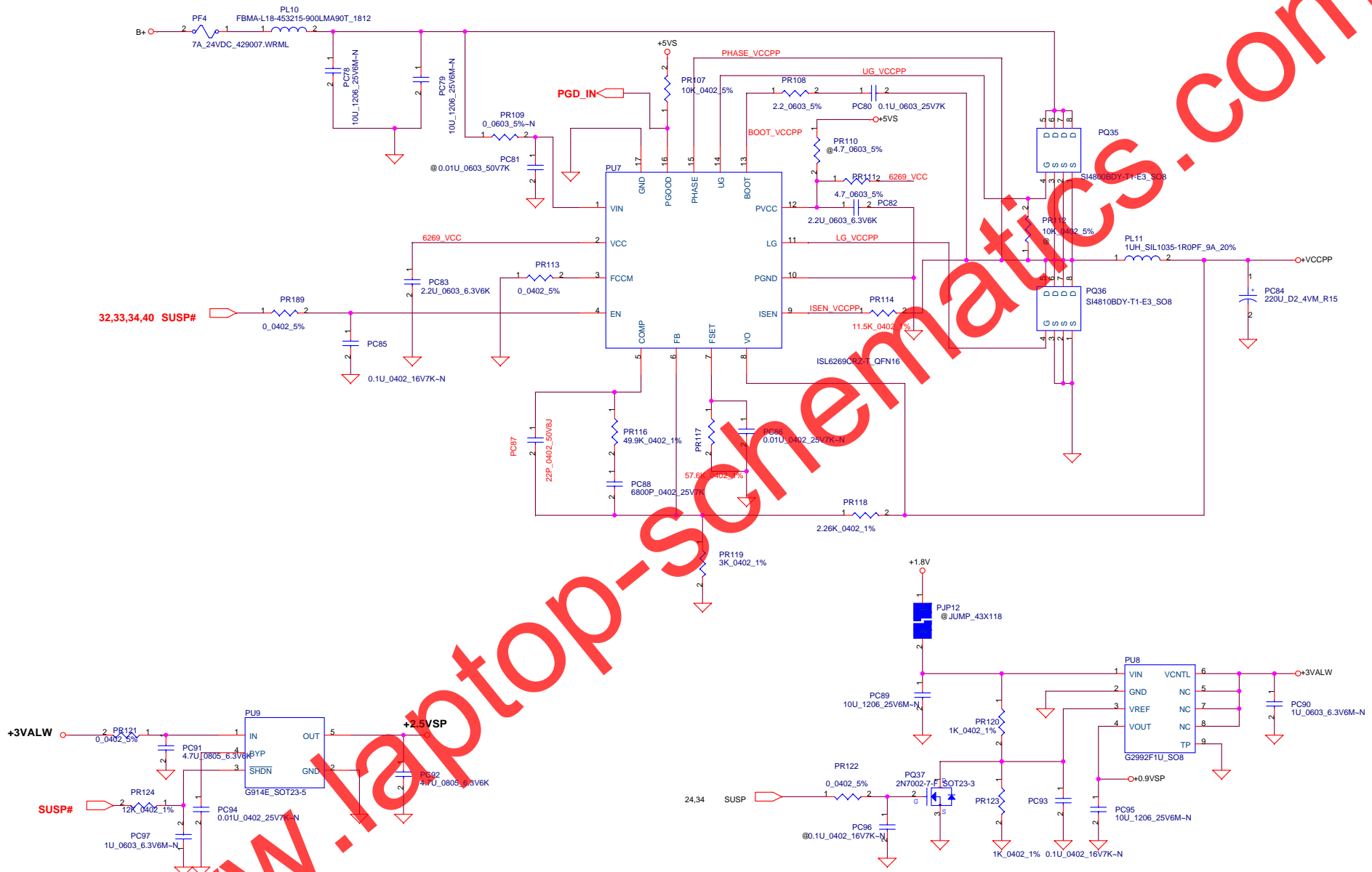
+3.3VALWP/+5VALWP

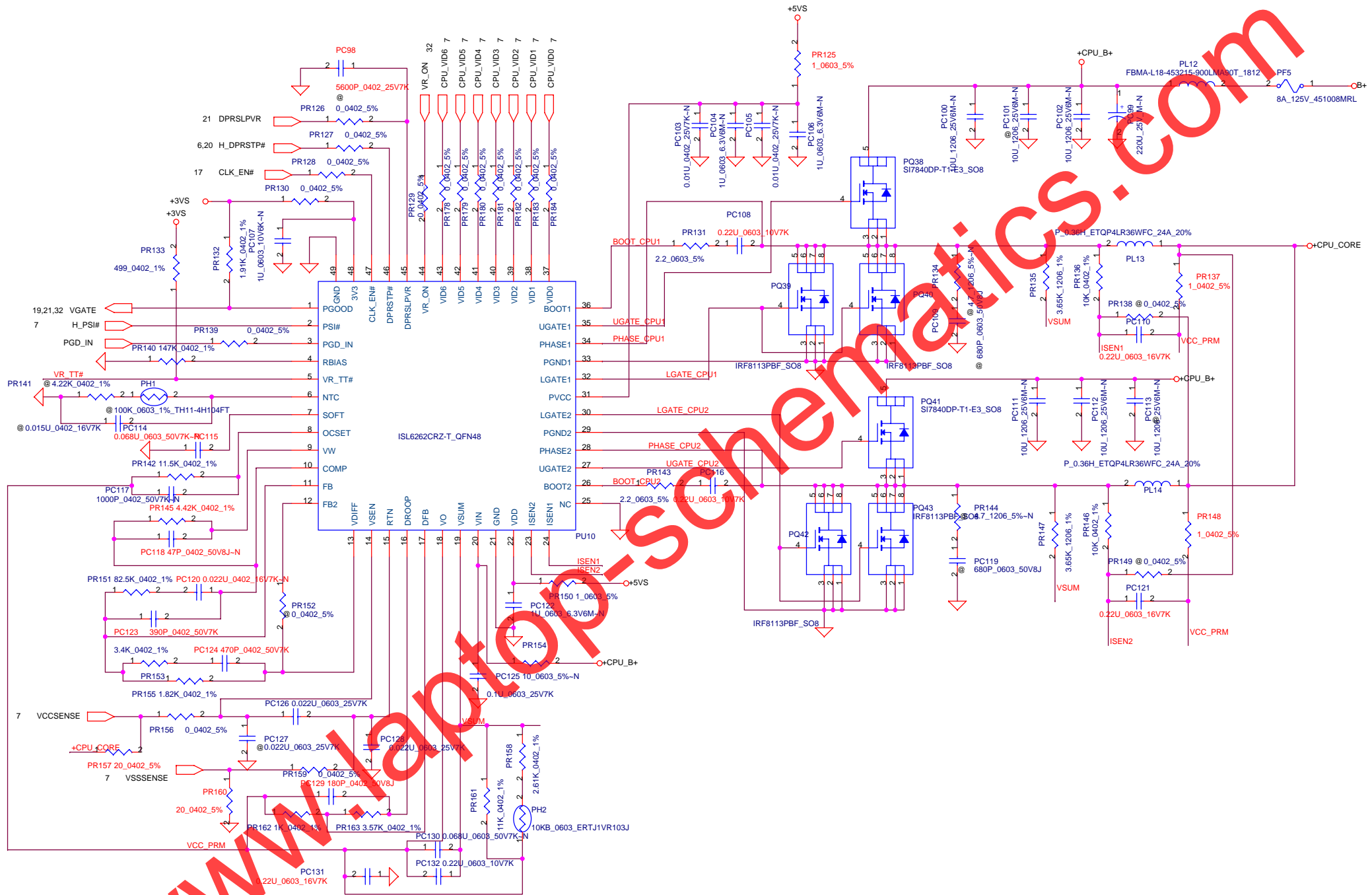


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www.laptopcircuitdiagramatics.com

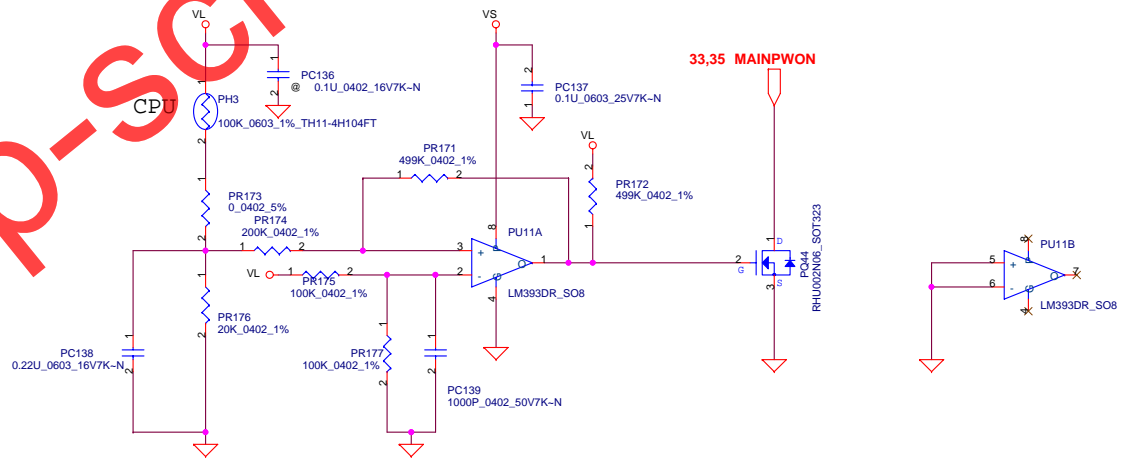
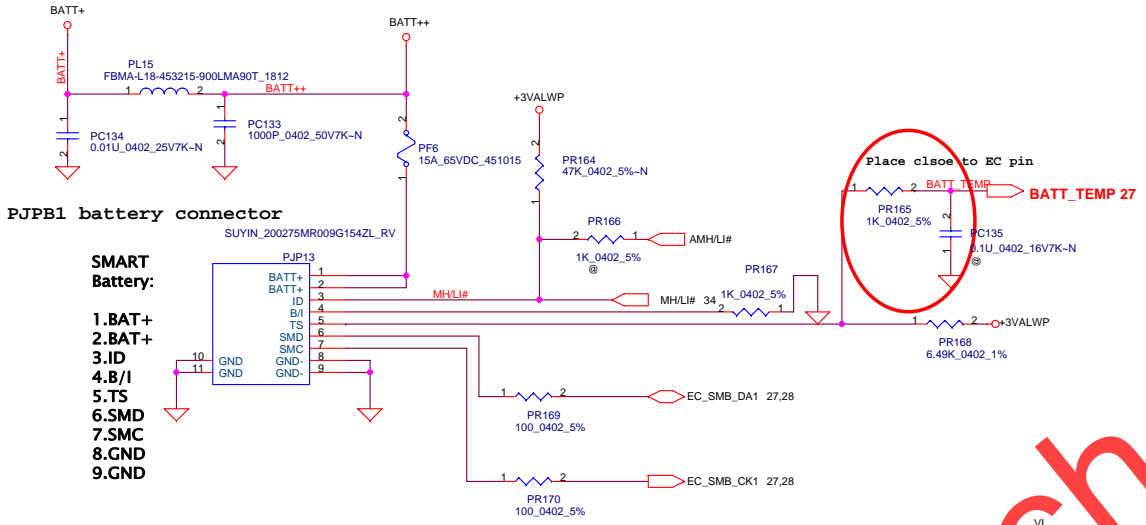






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Battery Connect/OTP



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